Updated !

ITRS
Design DTWG

November 30, 1999
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Tokyo, Japan

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"http://eda.ics.es.osaka-u.ac.jp/eiaj/eda/project/eda-vision.html "

Design Technology Issues

- Design systems are already at the breaking point in dealing with today' products because of:
  - Increasing complexity
    - Process complexity
    - Functional complexity (HW and embedded software)
    - System on a chip heterogeneity
  - Increasing frequency
  - Increasing importance of time-to-market ("Internet Time")
- Failure to address these issues directly will limit our ability to extract the full value from our manufacturing technology

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IC Design Roadmap

- Enable users of ICs to create products with the highest value using the current IC manufacturing technology
- Unlike other parts of the Roadmap, all advances in any area can be used to increase productivity and lower cost at any node.
  - No structured timeline of advances, it just gets easier or harder depending on the state of the tools.
  - Cost/difficulty of design will limit the ability to utilize IC manufacturing capability

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Superexponential Design Complexity

- Exponentially growing number of devices
- Design complexity is exponential function of device count

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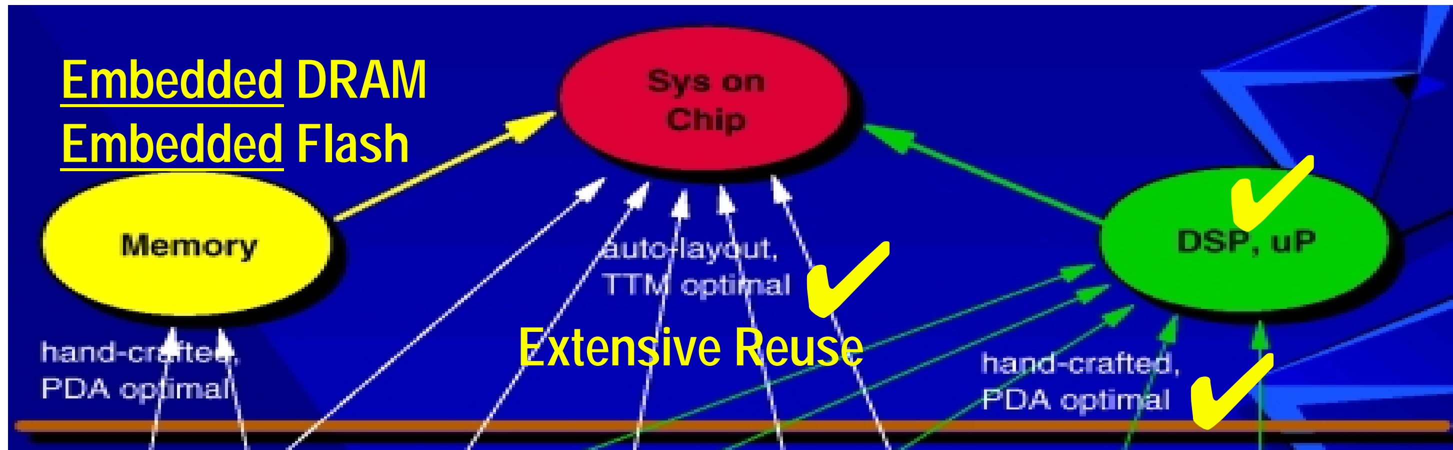
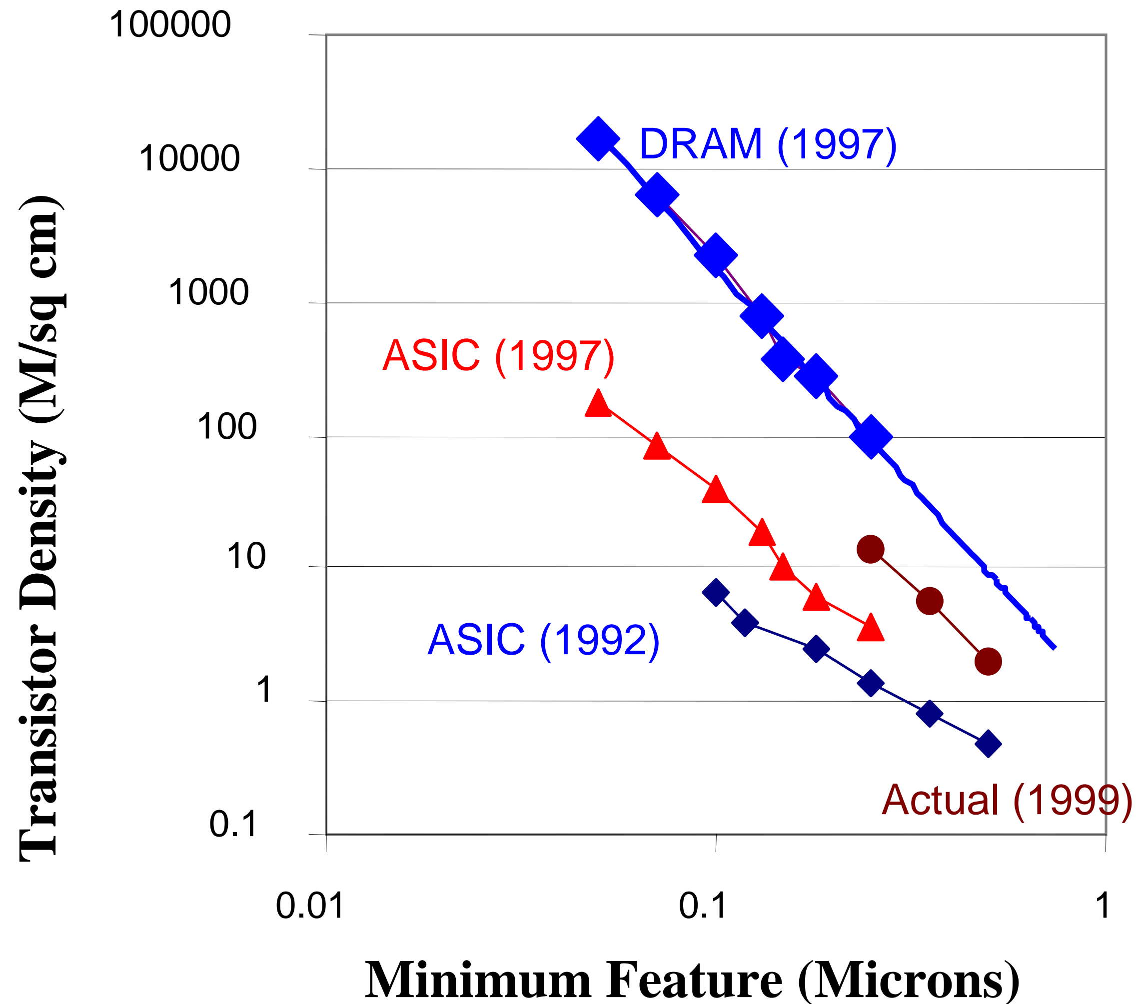
System-On-A-Chip Implies Mixed Technologies



ASIC Area Productivity Increases



ASIC densities have increased rapidly over last 3-5 years

New tools and MLM have brought density to 90% of max.

Future scaling will track DRAM

This puts even more pressure on design productivity

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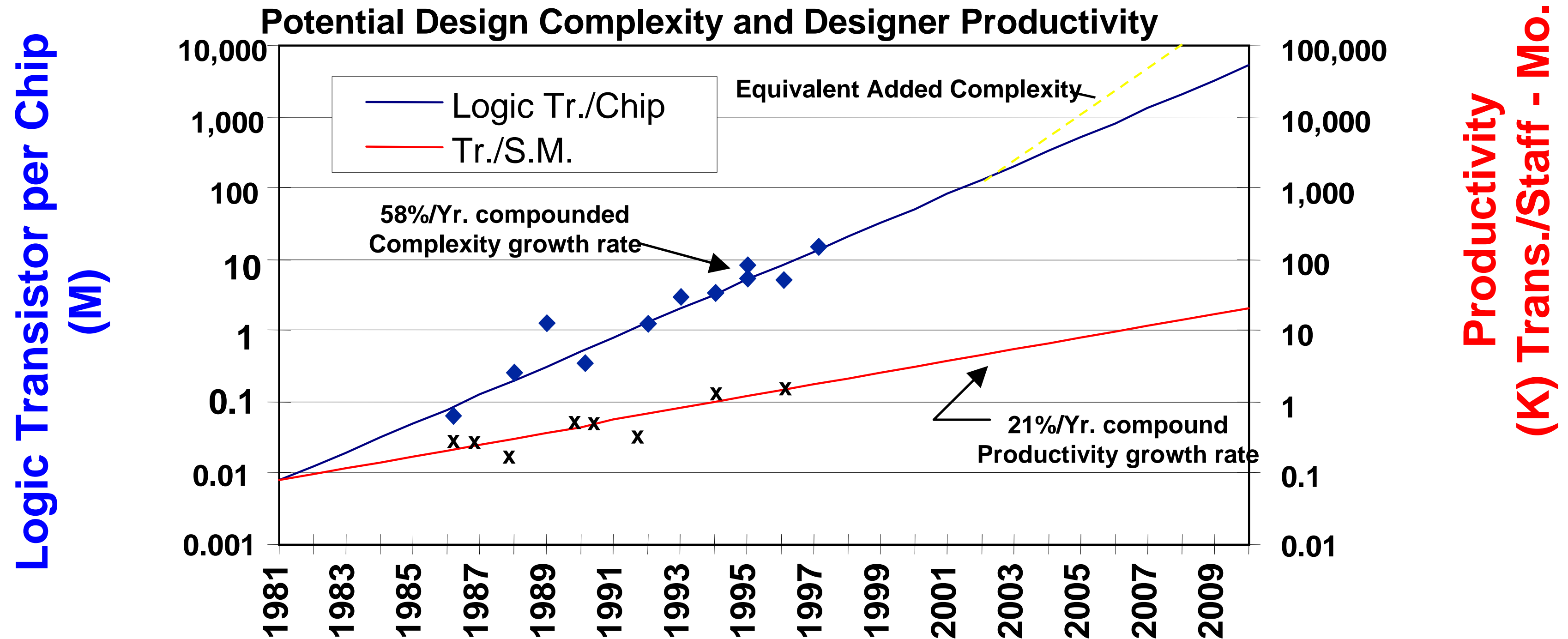
Design Productivity Crisis



Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / Staff Yr. (In 1997 Dollars)

Design Productivity and TTM Drive Revenue

- "Investment Theory 101"
  - Focus human CPU cycles on greatest return (Corollary: automate ***all*** else (or reuse))
  - ***Earliest*** design decisions have largest impact (Corollary: highest abstraction)
  - Products that miss market windows are dead (Corollary: Time-to-market is king)
- Raising working level of abstraction historically offers greatest leverage
  - Architecture, co-design, IP reuse
  - Requires ***bottoms-up*** feedback across flow

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International Technology Roadmap for Semiconductors

"Moore's Suggestion"

- It's NOT a fundamental law of physics
  - It's now a business proposal for investment
  - laws of physics may constrain its path
- It only works if revenue growth justifies the investment
- Memory density is no longer the driver
  - Objective function = (market value)/chip
  - Embedded software is a major component of the value
- ***Design productivity*** is the primary cost bottleneck moving forward
- This ***is*** a fundamental constraint arising from exploding complexity at all levels of the IC creation process

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International Technology Roadmap for Semiconductors

SOC Design Productivity Table

	Unit	1999	2002	2005	2011	
Technology Node	nm	180	130	100	50	
ASIC Usable Transistors	M Tr./cm2	20	54	133	811	(*1)
Logic gate count ratio in area	%	80%	50%	35%	15%	
Logic Gate count	M gates	4.00	6.75	11.64	30.41	
DRAM (Production)	M bits/cm2	200	525	1,230	7,510	(*1)
Embedded Memory size	M bits	16	105	319.8	2,553	
Power supply voltage	V	1.5	1.2	0.9	0.6	
Operation Frequency	MHz	150	400	1000	2000	
Design Resource	(ratio)	1	1.7	2.9	7.6	
Re-use circuit ratio	%	20%	50%	70%	90%	
Newly designed circuit	M gates	3.20	3.38	3.49	3.04	
Productivity improvement	%	100%	70%	49%	24.%	(*2)
Resource for Newly designed(A)	M gates	3.20	2.36	1.71	0.73	
Overhead in Re-use circuit	%	50%	35%	24%	12%	(*3)
Resource for Re-use circuit(B)	M gates	0.40	1.18	2.00	3.29	
Total Design resource(A+B)	M gates	3.60	3.54	3.71	4.02	
Target Design Resource	Man*Years	10	9.8	10.3	11.2	

(*1) ITRS'99 ORTC (*2) 30% off / 3 years improvement

(*3) 30% off / 3 years improvement

Design Difficult Challenges

≥ 100 NM (BEFORE year 2005)

Silicon complexity	System complexity	Design procedure complexity	Verification complexity
1. Large numbers of interacting devices and interconnects 2. Impact of signal integrity, noise, reliability, manufacturability Atomic-scale effects 3. Power and current management; voltage scaling 4. Need for new logic families to meet performance challenges 5. Atomic-scale effects 6. Alternative technologies (e.g. copper, low ?, SOI)	1. Embedded software as a key design problem 2. System-on-a-chip design with a diversity of design styles (including analog, mixed signal, RF, MEMS, electro-optical) 3. Increased system and function size 4. Use of open systems and incorporation into global networks 5. Integrated passive components	1. Convergence and predictability of design procedure 2. Core-based, IP-reused designs and standards for integration 3. Large, collaborative, multi-skilled, geographically distributed teams 4. Interacting design levels with multiple, complex design constraints 5. Specification and estimation needed at all levels 6. Technology remapping or migration to maintain productivity	1. Formal methods for system-level verification 2. System-on-a-Chip specification 3. Early high-level timing verification 4. Core-based design verification (including analog/mixed signal) 5. Verification of heterogeneous systems (including mixed-signal, MEMS)

< 100 NM (AFTER year 2005)

Silicon complexity	System complexity	Design procedure complexity	Verification complexity
1. Uncertainty due to manufacturing variability 2. Uncertainty in fundamental chip parameters (such as signal skew) 3. Design with novel devices (multi-threshold, 3D layout, SOI, etc.) 4. Soft errors	1. Total system integration including new integrated technologies (such as MEMS, electro-optical, electro-chemical, electro-biological) 2. Design techniques for fault tolerance 3. Embedded software and on-chip operating system issues	1. True one-pass design process supporting incremental and partial design specification 2. Integration of design process with manufacturing to address reliability and yield	1. Physical verification for novel interconnects (optical, RF, 3D) at high frequency 2. Verification for novel devices (nanotube, molecular, chemical)

Critical Challenges ≥ 100 nm

- **Silicon Complexity**
  - Large numbers of interacting devices and interconnects
  - Atomic-scale effects
  - Impact of signal integrity, noise, reliability, manufacturability
  - Need for new logic families to meet performance challenges
  - Power and current management; voltage scaling
  - Alternative technologies (e.g. copper, low K, SOI)

Critical Challenges $\geq$ 100 nm

- **System Complexity**
  - Greatly increased system and function size
  - System-on-a-chip design with a diversity of design styles (including analog, mixed signal, RF, MEMS, electro-optical)
  - Integrated passive components
  - Embedded software as a key design

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Critical Challenges ≥ 100 nm

- **Design procedure complexity**
  - Interacting design levels with multiple, complex design constraints
  - Convergence and predictability of design procedure
  - Specification and estimation needed at all levels
  - Technology re-mapping or migration to maintain productivity
  - Core-based, IP-reused designs and standards for integration
  - Large, collaborative, multi-skilled, geographically distributed teams

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Critical Challenges $\geq$ 100 nm

- **Verification and analysis complexity**
  - Early high-level timing verification
  - Formal methods for system-level verification
  - Core-based design verification (including analog/mixed signal)
  - Verification of complex processors and architectures
  - System on a chip specification
  - Verification of heterogeneous systems (including mixed signal, MEMS)
- **Test/testability complexity**
  - Quality and yield impact due to test equipment limits
  - Test of core-based designs from multiple sources (including analog, RF)
  - Difficulty of at-speed test with increased clock frequencies
  - Signal integrity testability

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Critical Challenges < 100 nm

- **Silicon complexity**
  - Design with novel devices (multi-threshold, 3D layout, SOI, etc.)
  - Soft errors
  - Uncertainty due to manufacturing variability
  - Uncertainty in fundamental chip parameters ()
- **System complexity**
  - Total system integration including new integrated technologies (e.g. MEMS, electro-optical, electro-chemical, electro-biological)
  - Design techniques for fault tolerance
  - Embedded software and on-chip operating system issues

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International Technology Roadmap for Semiconductors

Critical Challenges < 100 nm

- **Design procedure complexity**
  - True one-pass design process supporting incremental and partial design specification
  - Integration of design process with manufacturing to address reliability and yield
- **Verification and analysis complexity**
  - Physical verification for novel interconnects (optical, RF, 3-D, etc.)
  - Verification for novel devices (nanotube, molecular, chemical, etc.)
- **Test/testability complexity**
  - Dependence on self-test solutions for SOC (RF, analog, …)
  - System test (including MEMS and electro-optical components)

On-Chip Busses Limit MPU Performance

Speed Estimation

		Symbol	Unit	Equation	Source	1999	2001	2003	2005	2007	2009	Average
1/2 Pitch		A	nm	80%/2year	ITRS99	210	160	140	115	90	70	
Minimum Gate		B	nm	70%/2year	ITRS99	140	100	70	50	35	25	
Die Size		C	mm**2	11%/2year	ITRS99	340	374	411	453	498	548	
Gate Del	(*1)	D	ps	0.043 *B	DSM-WG	6.0	4.3	3.0	2.2	1.5	1.1	
RC Delay per Length	(*2)	E	ps/mm		DSM-WG	7.33	13.03	18.72	30.25	61.33	92.40	
	Wire Len	F	pitch		DSM-WG	100	100	100	100	100	100	
Delay of Block	Wire Del	G	ps	A*2*E*F	DSM-WG	0.3	0.4	0.5	0.7	1.1	1.3	
Internal Data Signal	Gate Del	H	ps	E	DSM-WG	6.0	4.3	3.0	2.2	1.5	1.1	
	Total	I	ps	G+H	DSM-WG	6.3	4.7	3.5	2.8	2.6	2.4	
	Improvemen	J	X/2year		DSM-WG		1.34	1.33	1.24	1.09	1.10	1.22
	Wire Len	L	pitch		DSM-WG	48000	48000	48000	48000	48000	48000	
Delay of Local Bus	Wire Del	M	ps	A*2*E*F	DSM-WG	147.8	200.1	251.6	334.0	529.8	620.9	
	Gate Del	N	ps	E	DSM-WG	6.0	4.3	3.0	2.2	1.5	1.1	
	Total	O	ps	G+H	DSM-WG	153.8	204.4	254.6	336.1	531.4	622.0	
	Improvemen	P	X/2year		DSM-WG		0.75	0.80	0.76	0.63	0.85	0.76

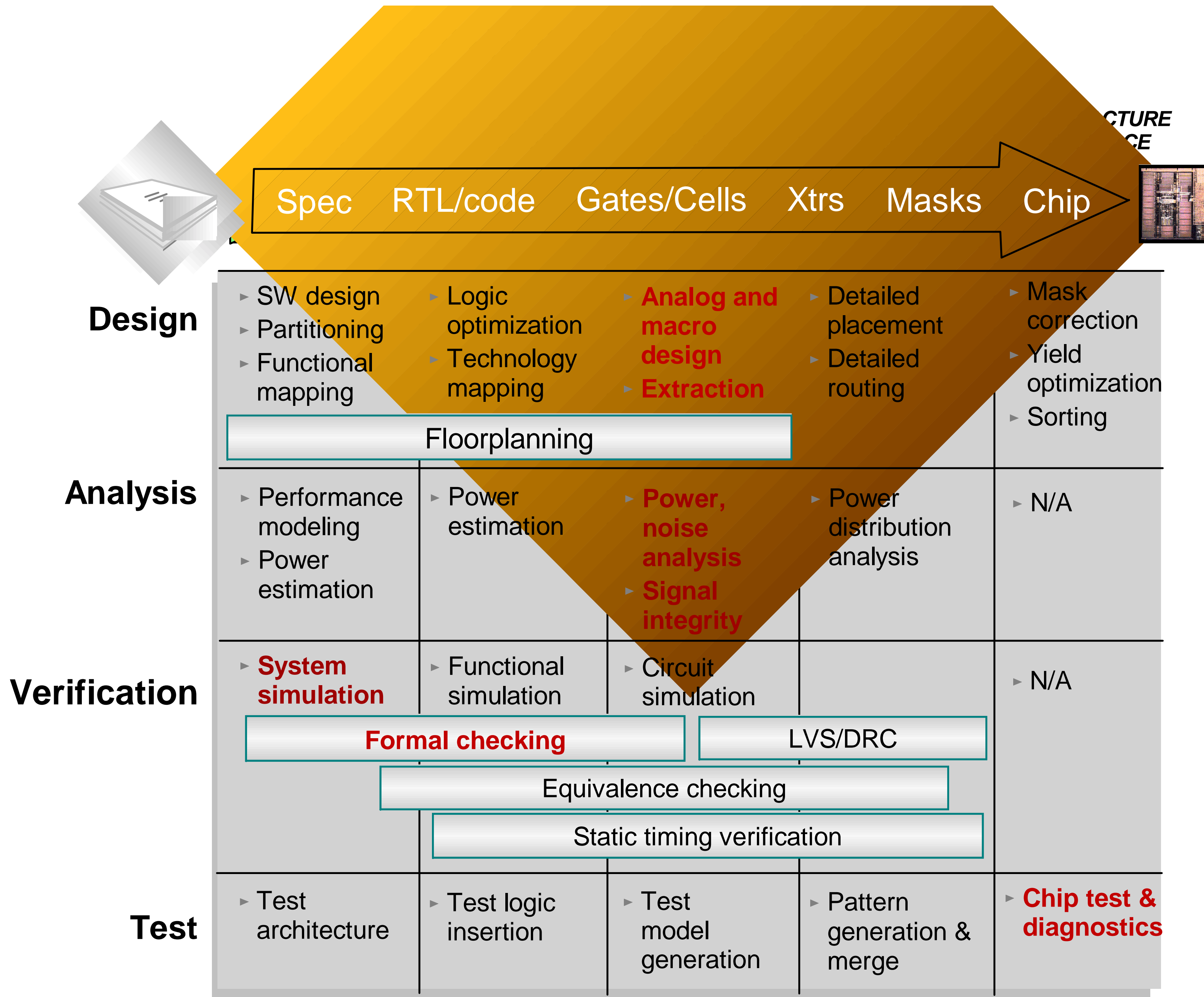
Busses getting slower!!

MPU Performance Estimation with DSM

Design architecture will be critical to recover performance loss due to interconnect

Performance Estimation

		Symbol	Unit	Equation	Source	1999	2001	2003	2005	2007	2009	Average
1/2 Pitch		A	nm	80%/2year	ITRS99	210	160	140	115	90	70	
Minimum Gate		B	nm	70%/2year	ITRS99	140	100	70	50	35	25	
Die Size		C	mm**2	11%/2year	ITRS99	340	374	411	453	498	548	
Transistors/Chip	Lithography	X	X/2year	1/(A**2)	ITRS99		1.7	1.3	1.5	1.6	1.7	1.56
	Chip Size	Y	X/2year	C	ITRS99		1.1	1.1	1.1	1.1	1.1	1.10
Delay of Block	Total	I	ps		DSM-WG	6.3	4.7	3.5	2.8	2.6	2.4	
Internal Data Signal	Improvemen	J	X/2year		DSM-WG		1.3	1.3	1.2	1.1	1.1	1.22
Local Bus Speed	Total	O	ps		DSM-WG	153.8	204.4	254.6	336.1	531.4	622.0	
	Improvemen	P	X/2year		DSM-WG		0.75	0.80	0.76	0.63	0.85	0.76
MPU Fr	ITRS99 Tar	Q	X/2year		ITRS99	1.2	1.2	1.2	1.2	1.2	1.2	
		R	MHz		DSM-WG	1250	1500	1800	2160	2592	3110	
	Allowable	S	MHz	1/(O*5)	DSM-WG	1300	979	786	595	376	322	
MPU Performance	Improvemen	Z1	X/2year	X*Y*J	DSM-WG		2.54	1.92	2.02	1.96	2.00	2.09
(Driven by Internal Data Signal)	Scaled Value	Z2			DSM-WG	1.00	2.54	4.87	9.87	19.33	38.72	
MPU Performance	Improvemen	Z3	X/2year	X*Y*P	DSM-WG		1.43	1.15	1.23	1.14	1.55	1.30
(Driven by Local Bus Speed)	Scaled Value	Z4			DSM-WG	1.00	1.43	1.64	2.03	2.31	3.58	



New Figure 4 (Draft Rev. B, 3-12-99)

Red denotes most challenging activity

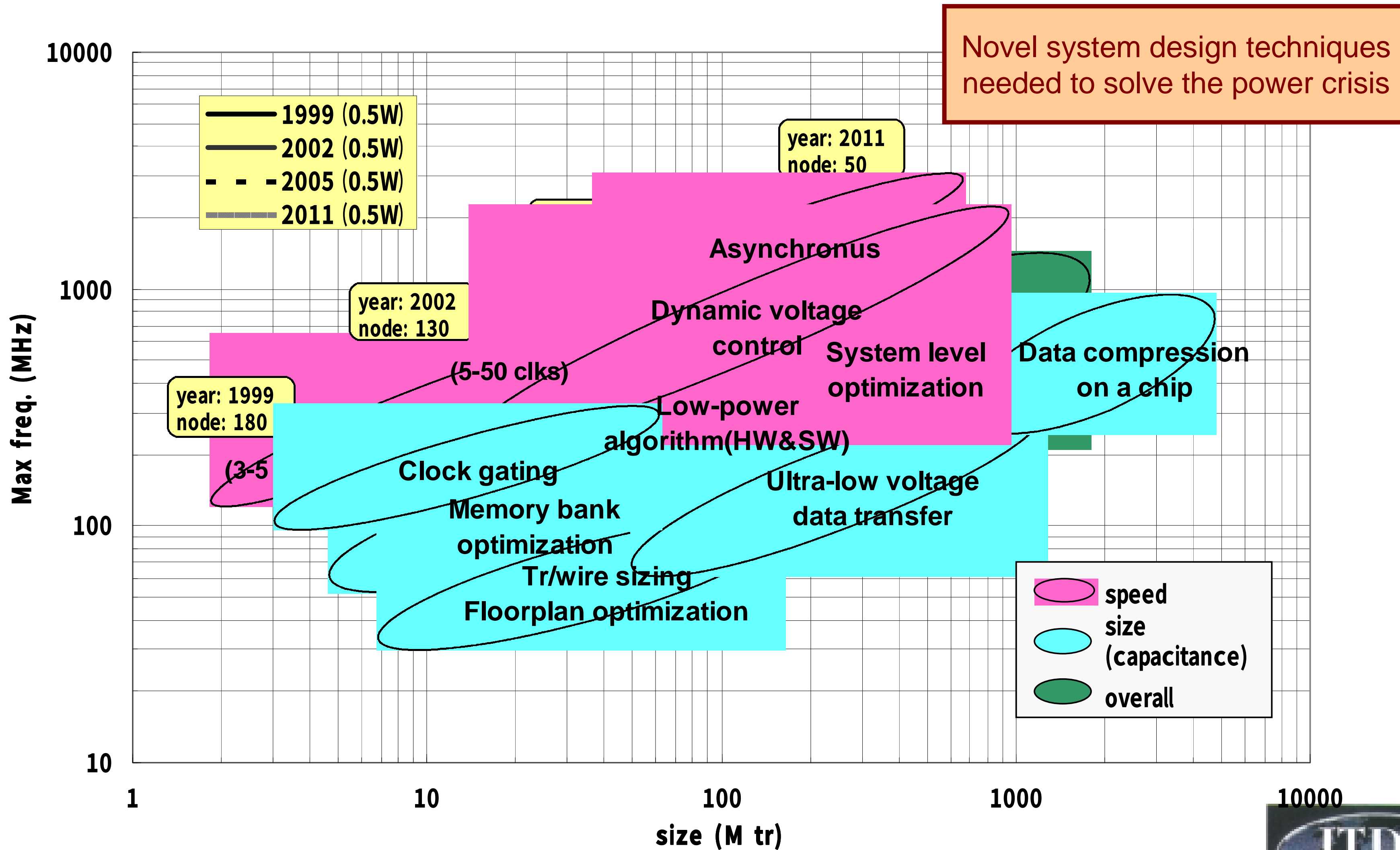
Power Trend Estimation

Design for low power concerns will dominate many portable IC applications

Design Parameters											
	unit	1999		2002			2005			2011	
technology node *	nm	180		130			100			50	
process factor		1.00	0.72	→	0.65	0.56	→	0.44	0.28	→	0.19
factor reduction	%	0			10			20			30
logic Tr count *	Mtr	16		27			46.55			121.7	
memory Tr count *	Mtr	16		100			319.8			2553.4	
total Tr *	Mtr	32		127			366.4			2675.1	
size factor(logic*1.0+mem*0.85)		1	3.78	→	1.89	10.76	→	4.30	77.43	→	23.23
factor reduction	%	0			50			60			70
max frequency	MHz	150		400			1000			2000	
frequency factor		1.00	2.67	→	2.00	6.67	→	3.33	13.33	→	5.33
factor reduction	%	0			25			50			60
internal voltage	V	1.5	1.2	→	1.0	0.9	→	0.6	0.5	→	0.3
voltage factor		1	0.64	→	0.44	0.36	→	0.16	0.11	→	0.04
voltage reduction	%	0			17			33			40
total power trend		1	4.66	→	1.09	14.34	→	1.02	31.87	→	0.96
power (estimation)	W	**3**	**13.99**	→	**3.28**	**43.02**	→	**3.06**	**95.60**	→	**2.89**
target	W	**0.5**		**0.5**			**0.5**			**0.5**	
Low Power Spec											
switching activity	%	1.8	2.66	→	2.61	2.7	→	2.67	1.85	→	0.96
external voltage	V	1.7〜5.0		1.2〜5.0			1.2〜5.0			0.9〜5.0	
battery	Wh/kg	120〜130		140〜150			200〜250			400〜500	

*: reference to Design Productivity Table

Potential Solutions for Low Power (0.5W/Chip)



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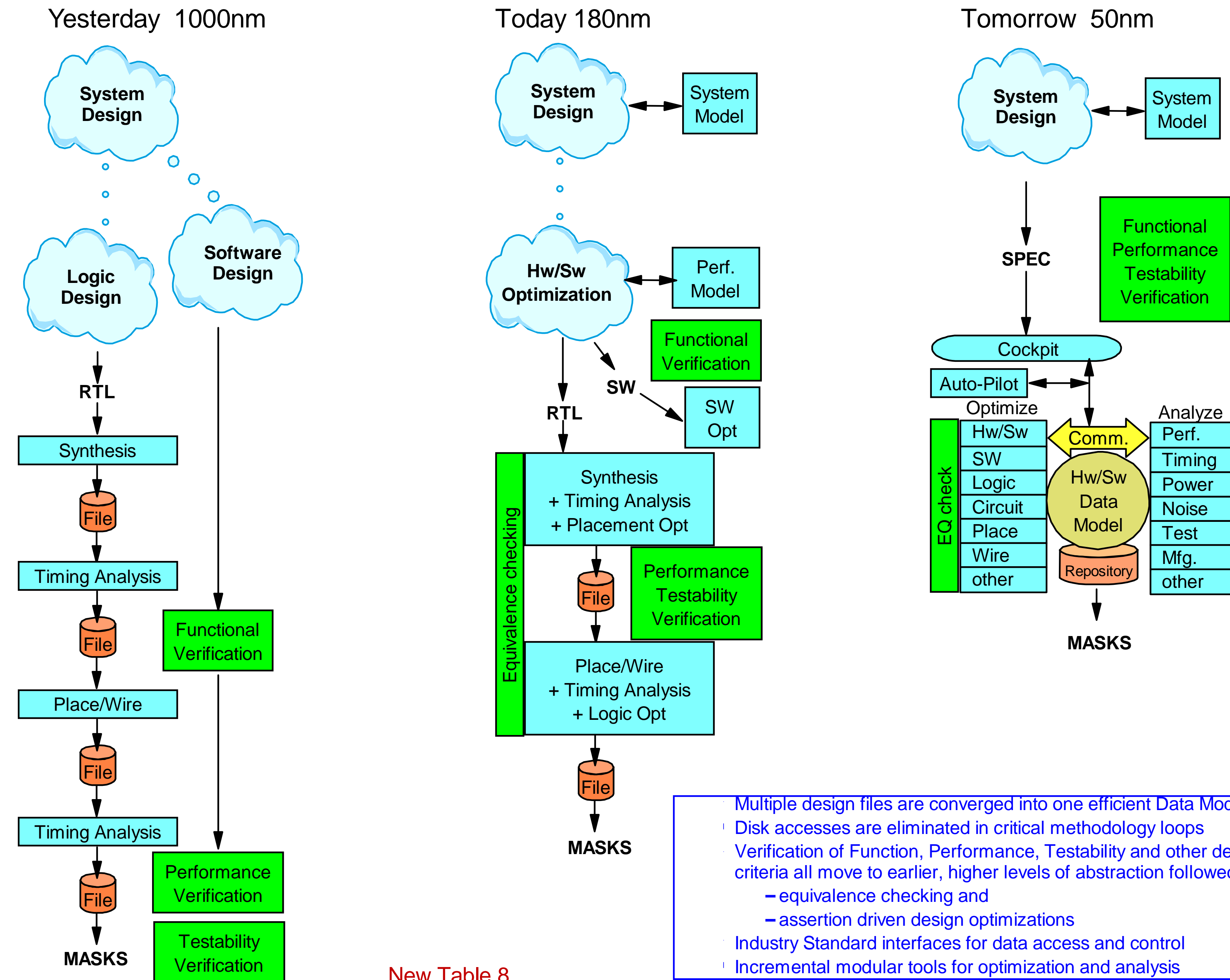
DSM Requirement Table

Category	Subcategory	Item	1999	2002	2005	2011
Base data/Condition			1999	2002	2005	2011
		Technology node (nm)	180	130	100	50
		Voltage (V)	1.5	1.2	0.9	0.6
		Frequncy (MHz)	150	400	1000	2000
		Die size (cm□)	1	1	1	1
		Metal height/width aspect		2.1	2.4	3
		Metal effective resistivity (μΩ-cmm)		2.2	2.2	<1.8
		Maximum metal current(mA)	2.16	1.56	1.2	0.6
DSM Category						
Signal Integrity	**Crosstalk noise** Required	Required parallel interconnect maximum allowable length which considers parastic capacitence effect (mm)	1.5	0.78	0.60	0.30
	Estimated	Estimated parallel interconnect maximum allowable length which considers parastic capacitence effect (mm)	5.33	0.21	0.00	0.00
	RC delay Required	Required interconnect maximum allowable length which considers resistence (mm)	10	10	10	10
	Estimated	Estimated interconnect maximum allowable length which considers resistence (mm)	454.5	66.7	16.5	2.7
	Inductance	Interconnect Inductance Effect			CP1 (*1)	CP2 (*2)
	EMI Allowed	Allowable EMI (*4) e.g.FCCclassB (uV/m at a distance of 3.0m)	150	200	500	500
	Estimated	Estimated EMI by a chip(obsavation point =3.0m) uV/m	11	22	43	43
Reliability	**IR drop** Required	Required maximum allowable number of FF which is driven by power line without failure due to IR Drop.	500	500	500	500
	Estimated	Estimated maximum allowable number of FF which is driven by power line without failure due to IR Drop.	736	267	172	78
	ElectroMigration	Number of Power Pads (High Performance)	241	317	470	714
		Number of Power Pads (Battery/Hand-Held)	4	6	9	11
		Number of Power Pads (Target of LP-SWG)	2	2	2	2
Manufacturebility	OPE	OPC			CP	

CP1(1st Crisis Point):Interconnect effects becomes critical in high speed blocks(1GHz).
CP2(2nd Crisis Point)Interconnect effects becomes major delay in high speed blocks(2GHz).

Required Advance in Design System Architecture



- Multiple design files are converged into one efficient Data Model
- Disk accesses are eliminated in critical methodology loops
- Verification of Function, Performance, Testability and other design criteria all move to earlier, higher levels of abstraction followed by
  - equivalence checking and
  - assertion driven design optimizations
- Industry Standard interfaces for data access and control
- Incremental modular tools for optimization and analysis

New Table 8

Design Technology Issues

- Design systems are already at the breaking point in dealing with today's products because of:
  - Increasing complexity
    - Process complexity
    - Functional complexity (HW and embedded software)
    - System on a chip heterogeneity
  - Increasing frequency
  - Increasing importance of time-to-market
- Failure to address these issues directly will limit our ability to extract the full value from our manufacturing technology

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