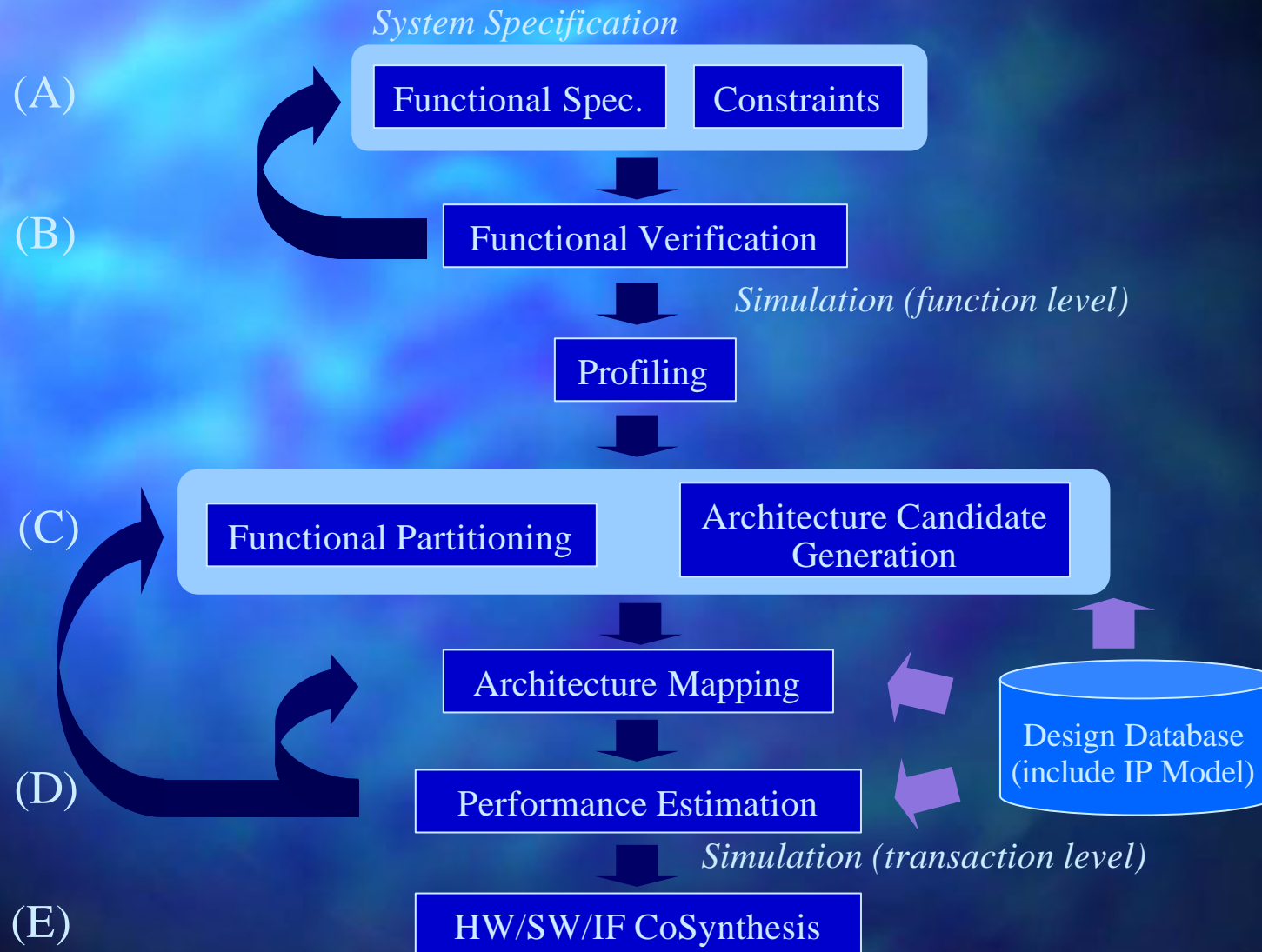


# System Level Design Flow proposed by SLD-SG

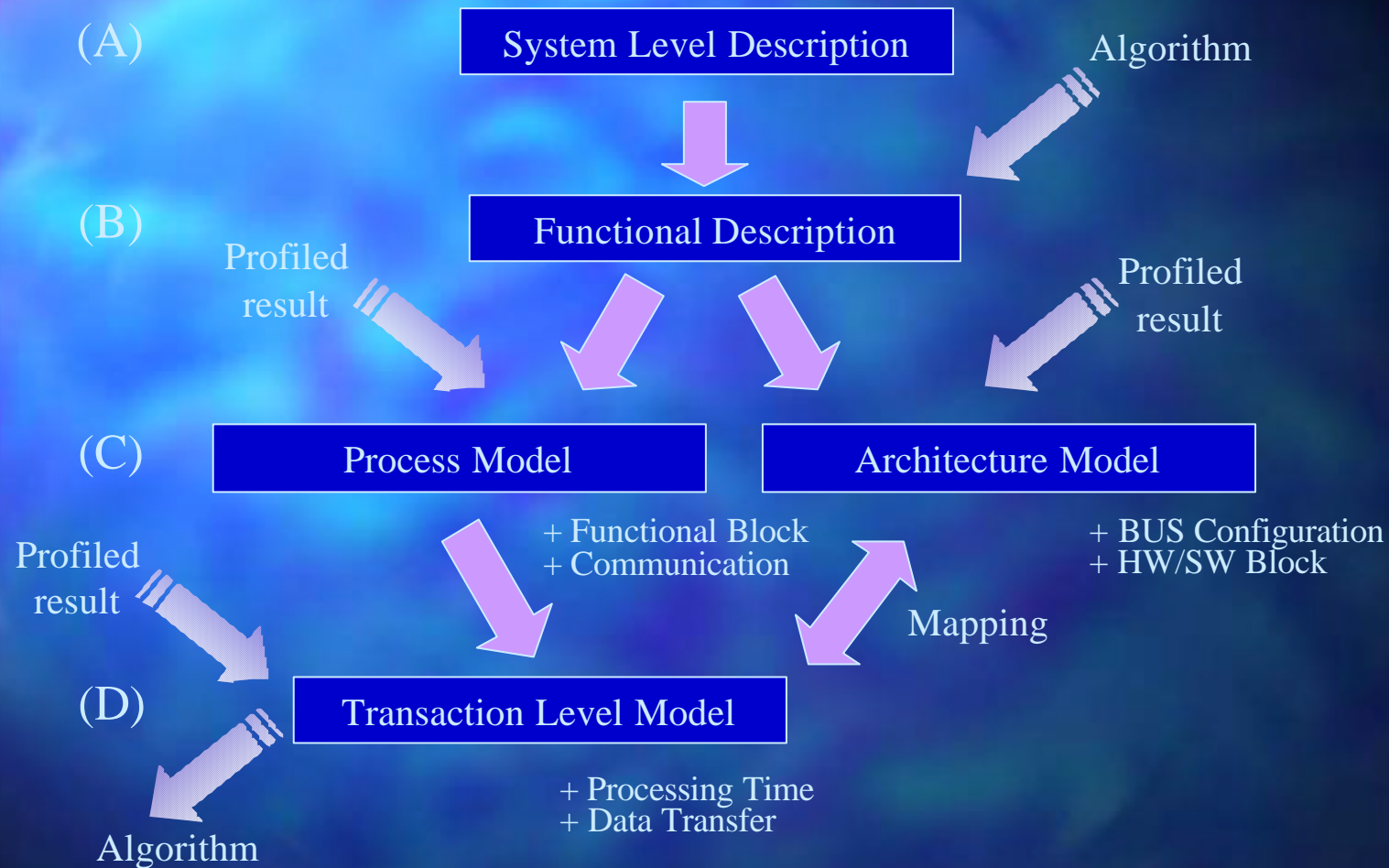
Masayoshi Tachibana  
(Toshiba Corp. Semiconductor Company)

Organized by EIAJ/EDA Technical Committee

# SLD Systems and Design Flow proposed by SLD-SG



# Description and Model



## SLD Systems and Design : What to DO

(A) & (B)

Define System Specification

*What to DO* : Describe required specification and design constraints

*Technology* : (Unified) System Level Description Language

System level verification technique

*Date* : 2000(?)

(C)

Functional Partitioning / Architecture Candidates Generation

*What to DO* : Generation of Architecture Candidates

Process modeling

Simulation and Profiling in functional level

*Technology* : Process model generation

Architecture model generation

*Date* : 2002~2003

## SLD Systems and Design : What to DO

(D)

### Architecture Selection

*What to Do* : Process-Architecture mapping

Performance estimation

*Technology* : Transaction level model generation

Process-Architecture mapping

Performance estimation

*Date* : 2002~2004

(E)

### Interface to Implementation phase

*What to Do* : HW/SW/IF CoSynthesis

*Technology* : Inter-process communication interface generation

HW/SW CoSynthesis

*Date* : 2004