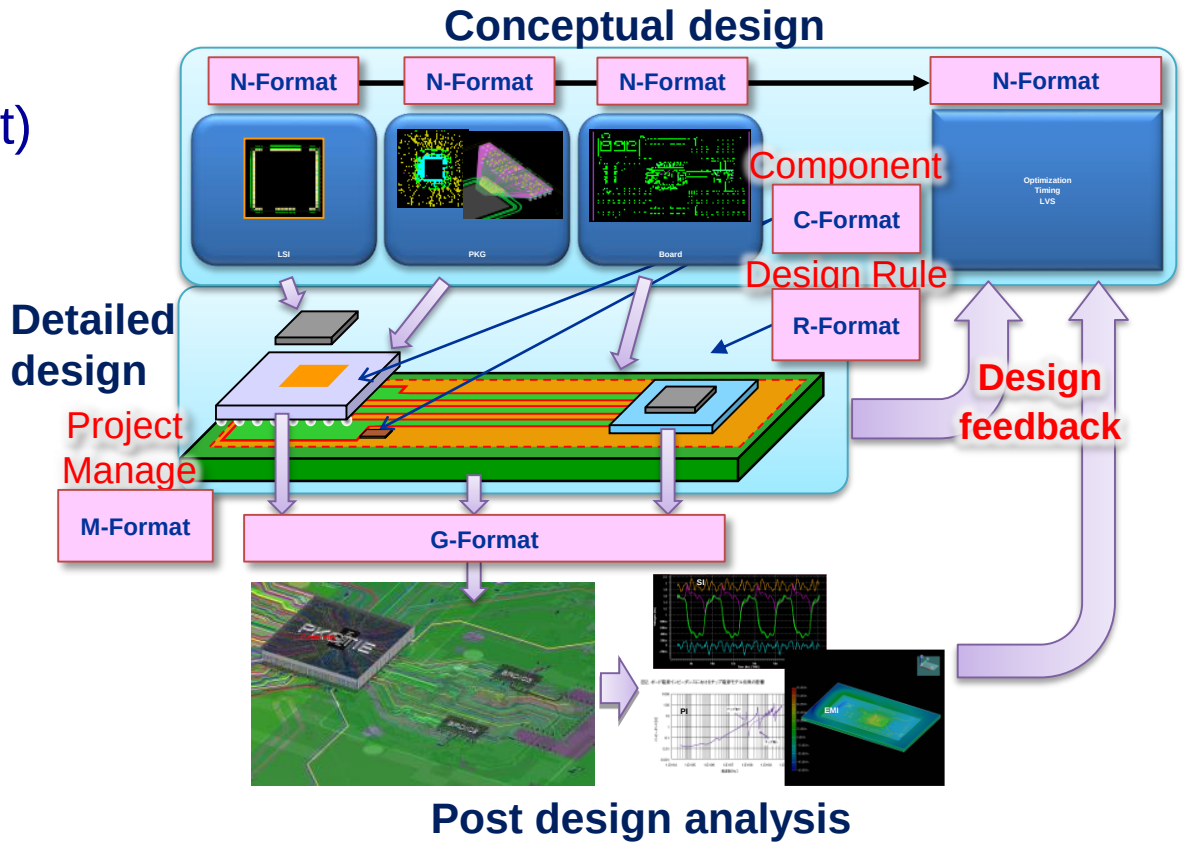
LPB Standard Format

Design environment to be constructed by 6 formats

1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary



LPB Standard Format Abstract

Format	Abstract	Benefit
Project Management (M-Format)	Manage the LPB files of the LSI, package and board. - Manage the history , revision and update of the files - JEITA original format using XML	Easy to Manage Design history Easy to understand Design Status Understanding The Latest Condition for Verification
Netlist (N-Format)	Connection of the parts - Netlist between LSI, Package and Board. - Verilog HDL format	Easy to Check Connection Between LSI-PKG-Board Enable to Simulate on Board Level
Component (C-Format)	Information of the parts that includes - Pin assignment - Design constraint - Design Status - JEITA original format using XML	Easy to Verify for Optimization of LPB Clarification of Constraint Condition
Design Rule (R-Format)	Rules of the components that includes - Design rule - Assembly rule - Characteristics of the material - JEITA original format using XML	Clarification of Design Rule in Advance Clarification of Verification Condition Easy to Set up for Verification
Geometry (G-Format)	Geometry of the Package and Board - XFL format	Efficient Use of Design Property Use as Reference Design Easy to convert Data

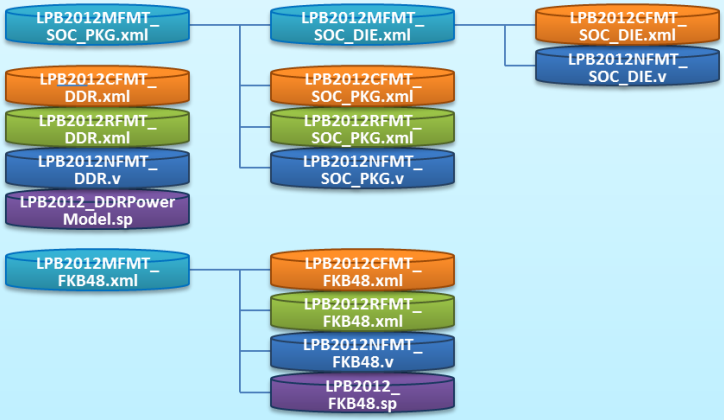
LPB Standard Format Abstract

Project Manage (M-Format)

Abstract

Manage the LPB files of the LSI, package and board.

- Manage the history , revision and update of the files
- JEITA original format using XML



Example

```
<include MFORMAT="MFMT_FKB48.xml" />
<include MFORMAT="MFMT_SOC_PKG.xml" />

<class comment="DDR MEMORY" >
  <CFORMAT   file_name="CFMT_DDR.xml" />
  <RFORMAT   file_name="RFMT_DDR.xml" />
  <NFORMAT   file_name="NFMT_DDR.v" />
  <OtherFile file_name="DDRPowerModel.sp" />
</class>
```

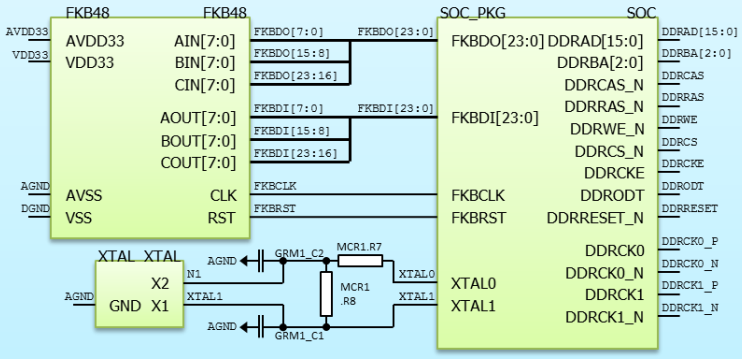
LPB Standard Format Abstract

Netlist (N-Format)

Abstract

Connection of the parts

- Netlist between LSI, Package and Board.
- Verilog HDL format



Example

```
module JEITA_SAMPLE ( );
    wire [23:0] FKBDO ;
    wire [23:0] FKBDI ;
    wire VDD33 ; /* PG_NET */
    wire DGND ;  /* PG_NET */

    FKB48 FKB48 ( .AIN(FKBDO),    .AOUT(FKBDI) ) ;
    SOC_PKG SOC ( .FKBDO(FKBDO), .FKBDI(FKBDI) ) ;

endmodule
```

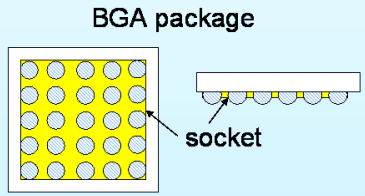
LPB Standard Format Abstract

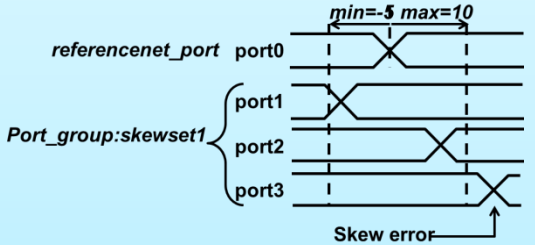
Component (C-Format)

Abstract

Information of the parts that includes

- Pin assignment
- Design constraint
- Design Status
- JEITA original format using XML





Example

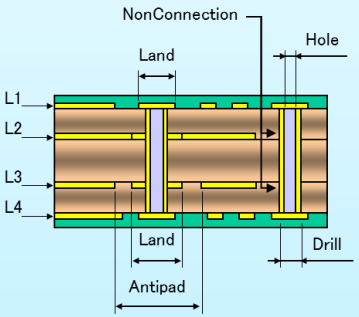
```
<module name="SOC_PKG" type="PKG" shape_id="PKG_BODY" >
  <socket  name="SOC_PKG" >
    <port  id="A5"    x="-8500"   y="12500"   angle="0"  name="FKBDO[5]" />
    <port  id="A6"    x="-7500"   y="12500"   angle="0"  name="FKBDO[2]" />
    <constraint>
      <impedance group_name="FKB_DIN"  type="single" min="40" typ="50" max="60"/>
      <delay     group_name="FKB_DIN"  min="100" typ="150" max="200" />
    </constraint>
  </socket>
</module>
```

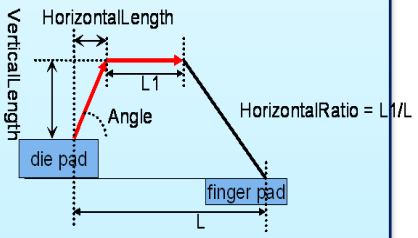
LPB Standard Format Abstract

Design Rule (R-Format)

Abstract

Rules of the components
- Design rule
- Assembly rule
- Characteristics of the material
- JEITA original format using XML



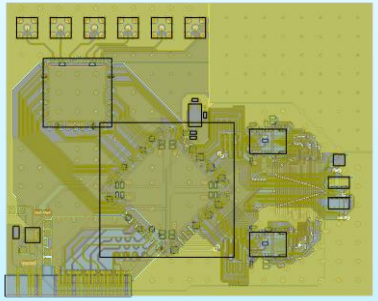


Example

```
<material_def>
  <conductor  material="COPPER" volume_resistivity="1.68e-8" />
  <dielectric material="FR-4"   permittivity="4.5"  tan_delta="0.035" />
</material_def>
<layer_def>
  <layer name="TOP_COND"  type="conductor"  thickness="0.030"
                          conductor_material="COPPER" />
  <layer name="DIELECTRIC12" type="dielectric" thickness="0.100"
                          dielectric_material="FR-4" />
</layer_def>
<spacing_def>
  <layer name="TOP_COND">
    <line_to_line  space="0.050" />
  </layer>
</spacing_def>
```

LPB Standard Format Abstract

Geometry (G-Format)

Abstract	Geometry of the Package and Board - XFL format 

Example	`shape 1 4 53.2 26.8 90 N`
	`via 1 4 V020C060C085 54.55 20 0 N`
	`via 2 3 B010C050C075C23 41 24.25 0 N`
	`shape 1 11 35.5 29 0 N`
	`via 1 2 B010C030C12 35.5 29 0 N`
	`path 2 0.1 {`
	`  41 24.25`
	`  41.000000 24.750000`
	`}`

LPB Files Delivery