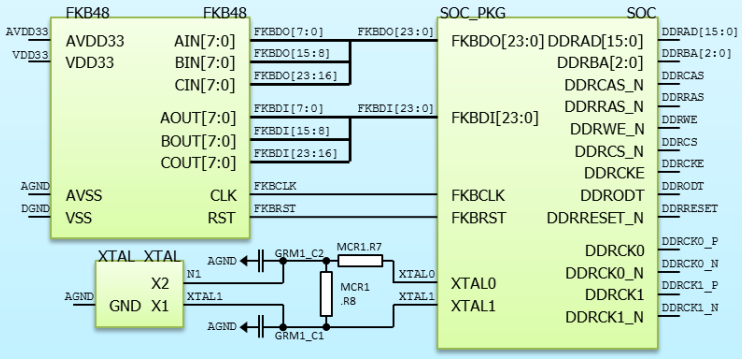
LPB Standard Format Abstract

Netlist (N-Format)

Abstract

Connection of the parts

- Netlist between LSI, Package and Board.
- Verilog HDL format



Example

```
module JEITA_SAMPLE ( );
    wire [23:0] FKBDO ;
    wire [23:0] FKBDI ;
    wire VDD33 ; /* PG_NET */
    wire DGND ;  /* PG_NET */

    FKB48 FKB48 ( .AIN(FKBDO),    .AOUT(FKBDI) ) ;
    SOC_PKG SOC ( .FKBDO(FKBDO), .FKBDI(FKBDI) ) ;

endmodule
```