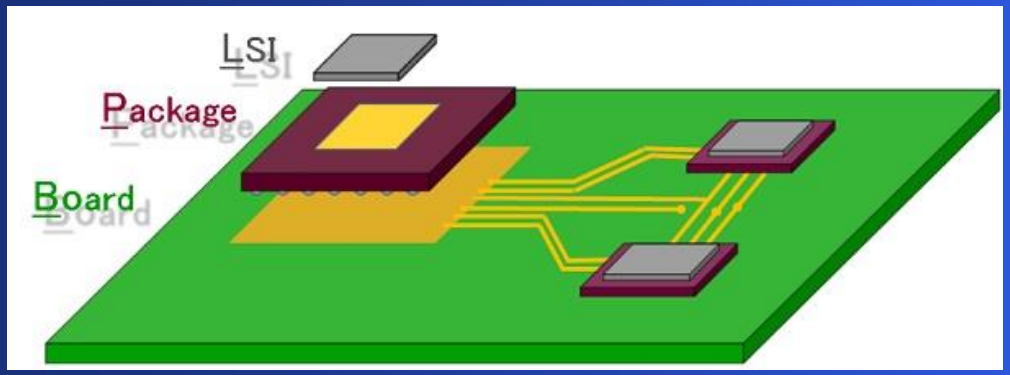
LSI Package Board needs…

- Mutual Communication
- Design Consistency
- Shorten Development Time

Enabled by

LPB *New Standard format*



Agenda & Speakers

- Introduction
  - Yoshinori Fukuba TOSHIBA
- LPB Standard Format
  - Yuji Nakagawa Fujitsu
- EDA - example of design tool
  - Kazunari Koga Zuken
- EDA – example of modeling/simulations
  - Toru Watanabe ANSYS
- Summary : Benefits
  - Yoshinori Fukuba TOSHIBA

Introduction of Fukuba

- Yoshinori Fukuba
  - Chief specialist, Design Technology Development dept., Mixed Signal IC Dev., TOSHIBA corporation Semiconductor & Storage
  - Chairman JEITA EDA-TC/LSI Package Board(LPB) interoperable design process WG(LPB-WG)

Today

  - Chairman IEEE Standard Association, Computer Society, Design Automation, Project : P2401 LPB-WG
  - Secretary IEC SC47A Integrated circuit

EMC

About LPB-WG

JEITA
Japan Electronics and Information Technology Industries Association

JEITA-JSIA Semiconductor board

JEITA EDA-TC Electronic Design Automation Technical Committee

LPB **LPB(LSI Package board) interoperable design process working group**

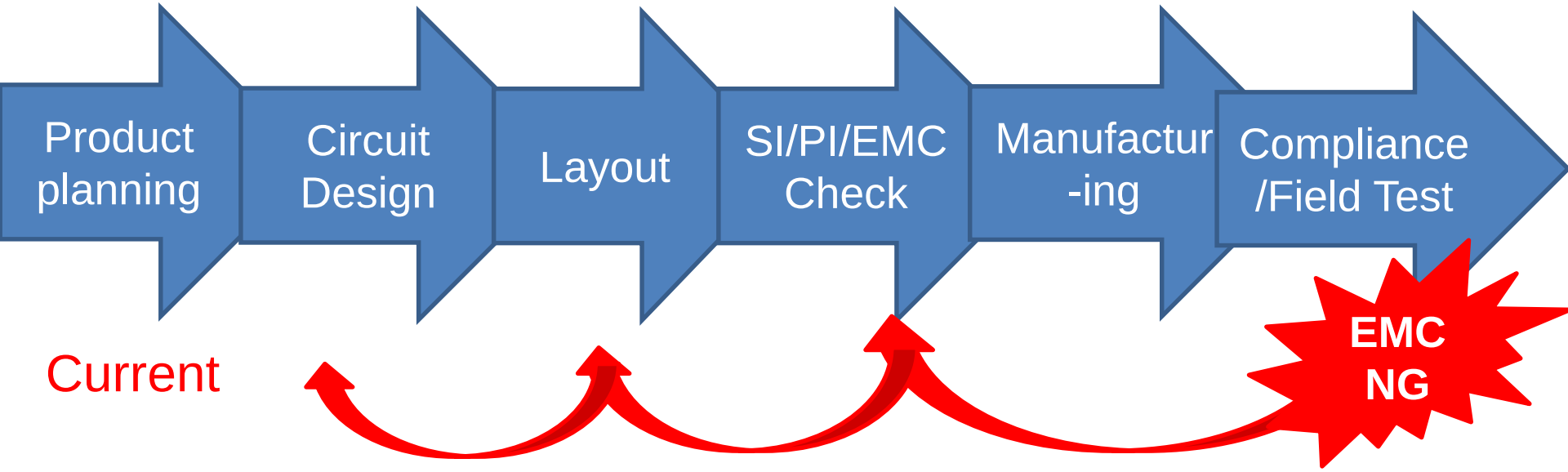
http://www.jeita-edatc.com/wg_lpb/home/lpb-en.html

- Members
  - LPB-WG + ex-LPB-WG

Toshiba, Fujitsu semiconductor, Renesas Electronics
Canon, Sony, Panasonic, Denso, Nokia
Fujitsu VLSI, Sony LSI, NEC System Technologies
Toppan NEC Circuit solutions
Zuken, Cadence Japan, Mentor Graphic Japan, StayShift(nimbic)
Fujitsu Advanced Technologies, Gem Design Technologies.
ANSYS, ANSYS Apache, ATE service(Sigrity) Else,

Issues

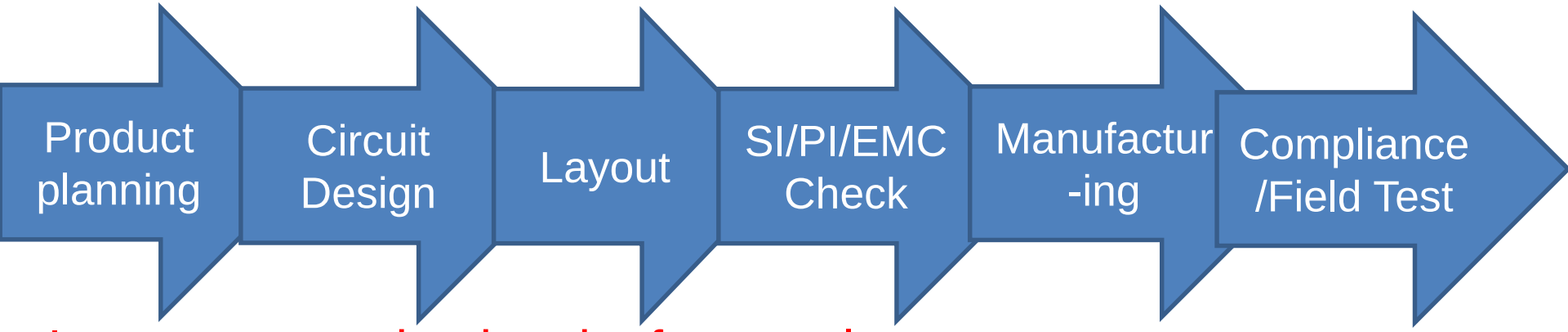
- Product development flow & EMC issues



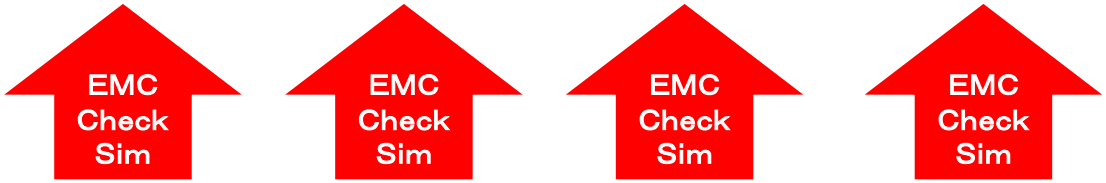
Time consuming, re-design at all
=>development cost,
missing business widow

Target to improve

- How to improve…



Improve - put check point from early stage,

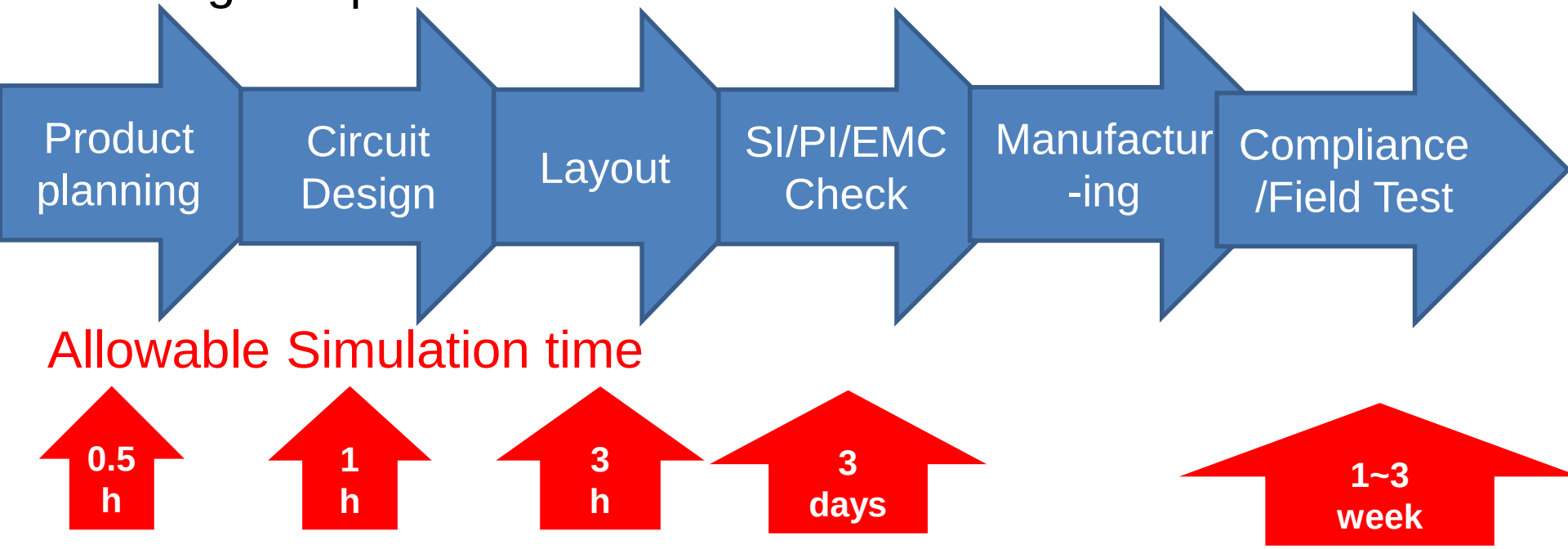


EMC issues Free

Reduce iterations
=>Time to market

Challenge of EMC simulation in design

- To estimate simulation time which is allowed in each design steps

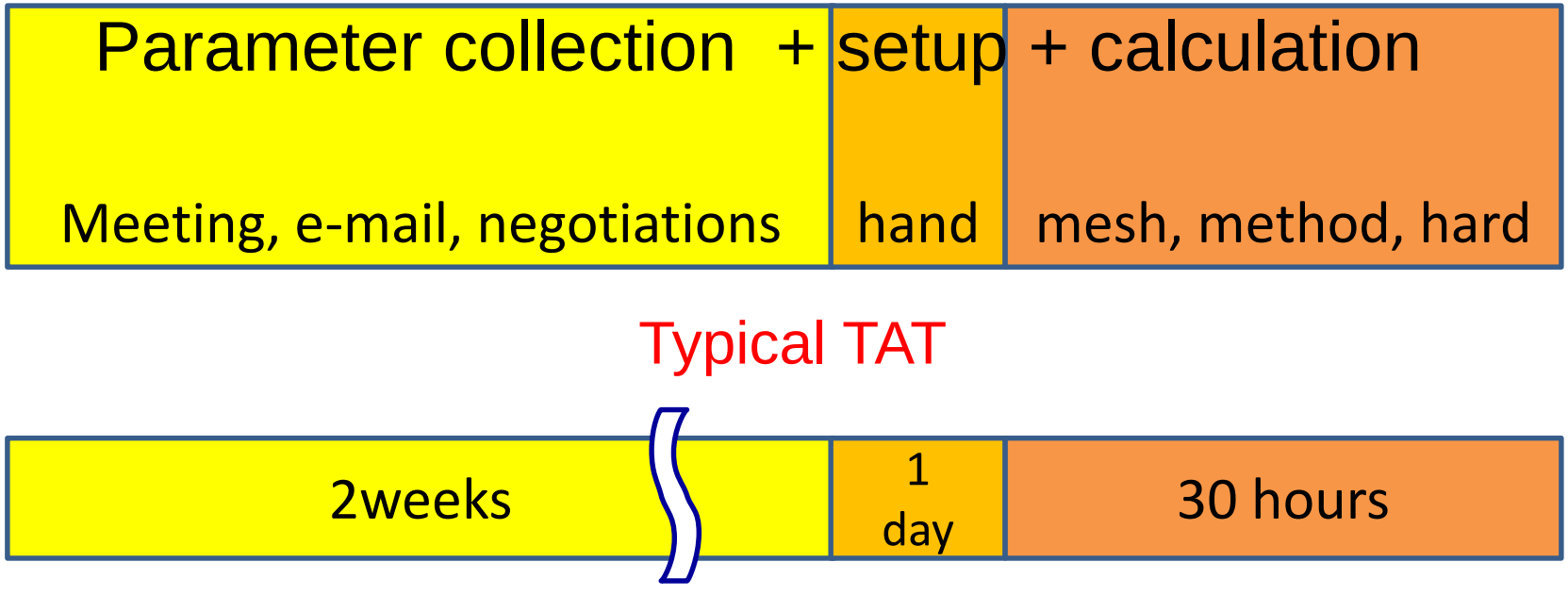


Allowable simulation times are different in the development stage.

What is the simulation time?

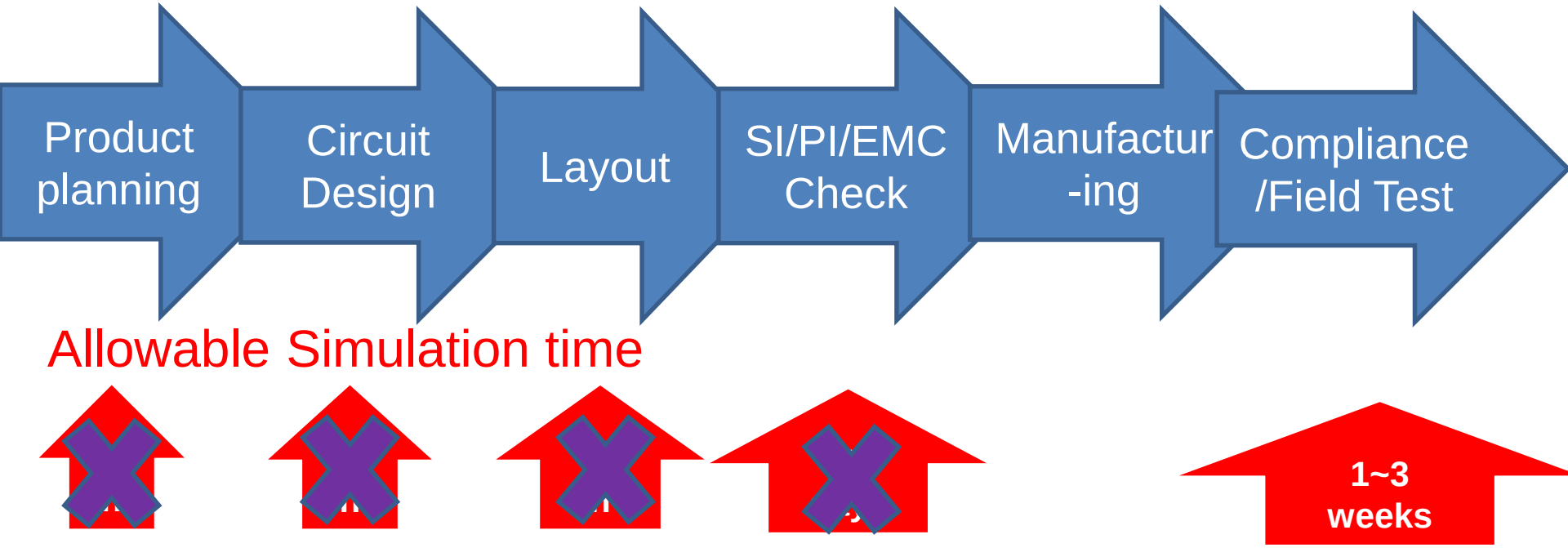
- definition

Simulation time =



However…

- Actually …



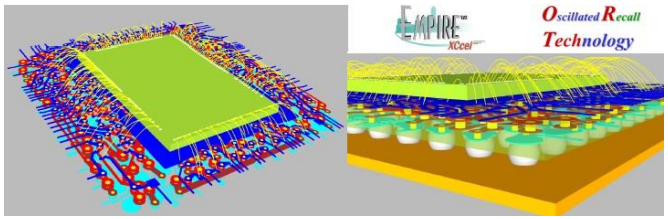
EMC simulation cannot be done at early stage.

Challenge to reduce the time. But…

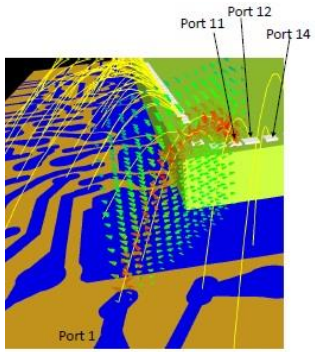
Parameter collection	setup	calculation
Meeting, e-mail, negotiations	hand	mesh, method, hard
2weeks	1 day	

X10~ X100

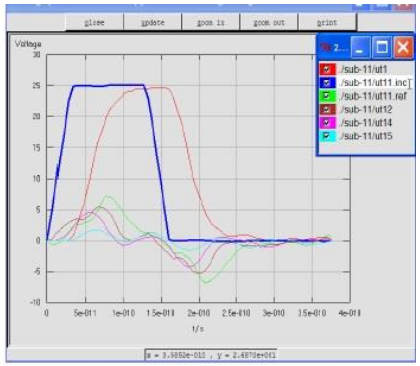
EDA / computer / Academic challenge



supplied by OR tech



3D view: Port definition

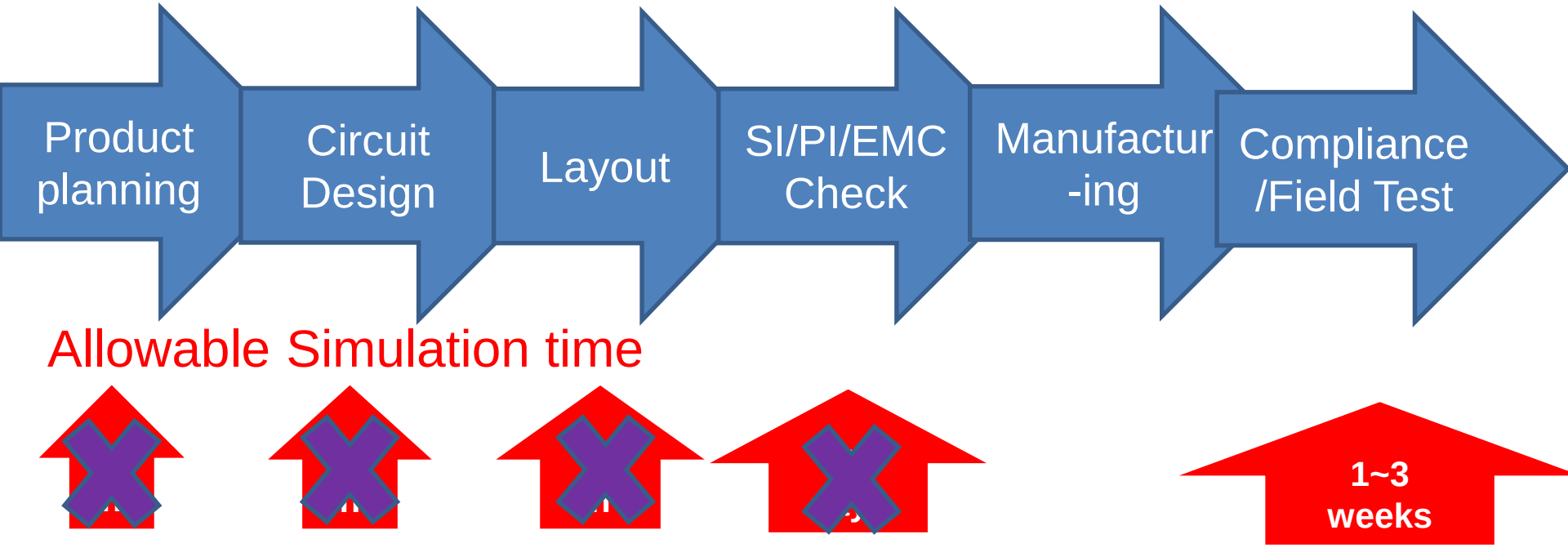


Test pulse excited at port 11

- Simulation time < 97sec / port ; Memory usage 680 MB
- 13 Million cells; grid: 15 µm < Δ < 200 µm
- Used CPU: Intel Xeon E5-2687W

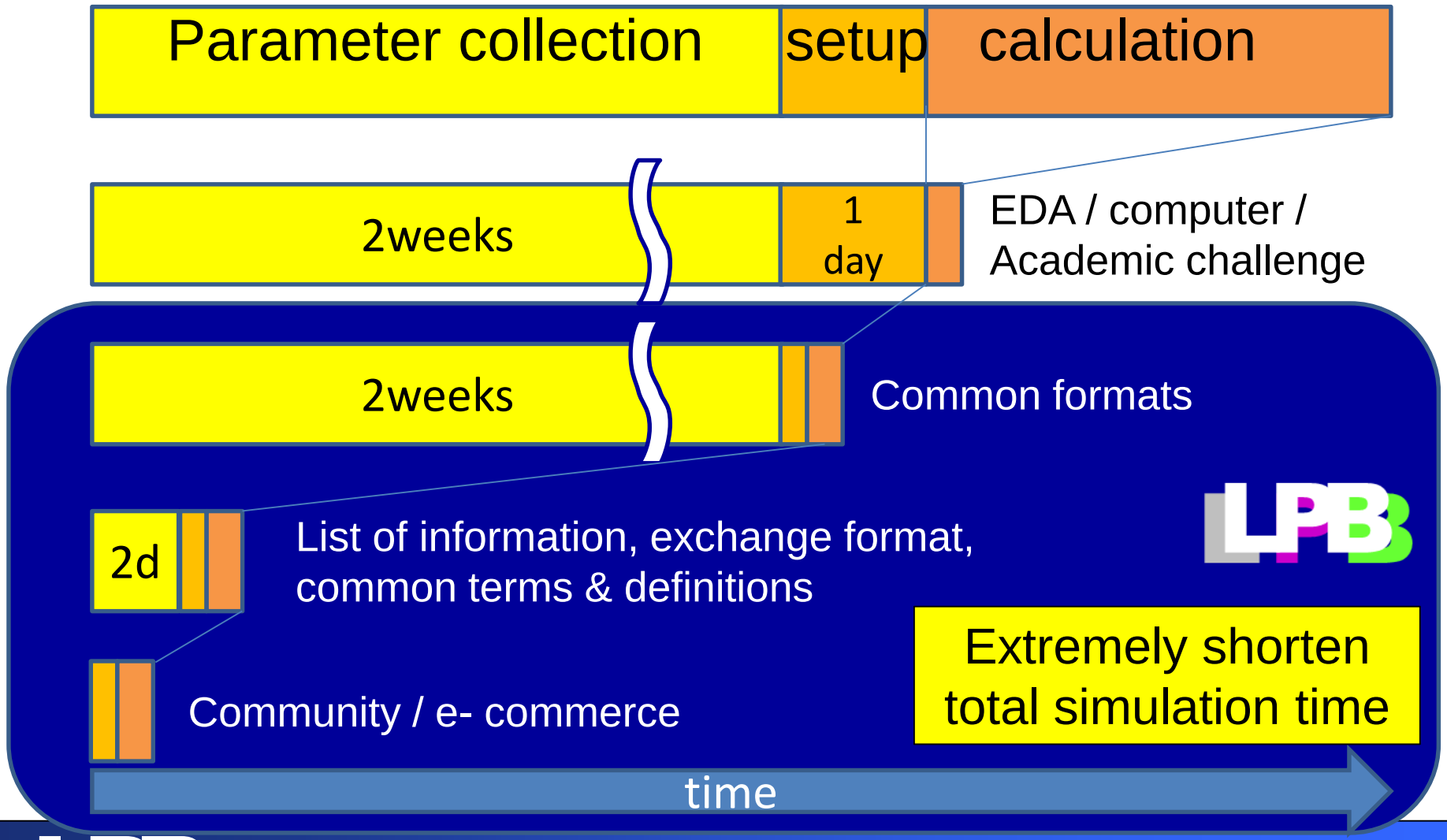
Still…

- Not enough …



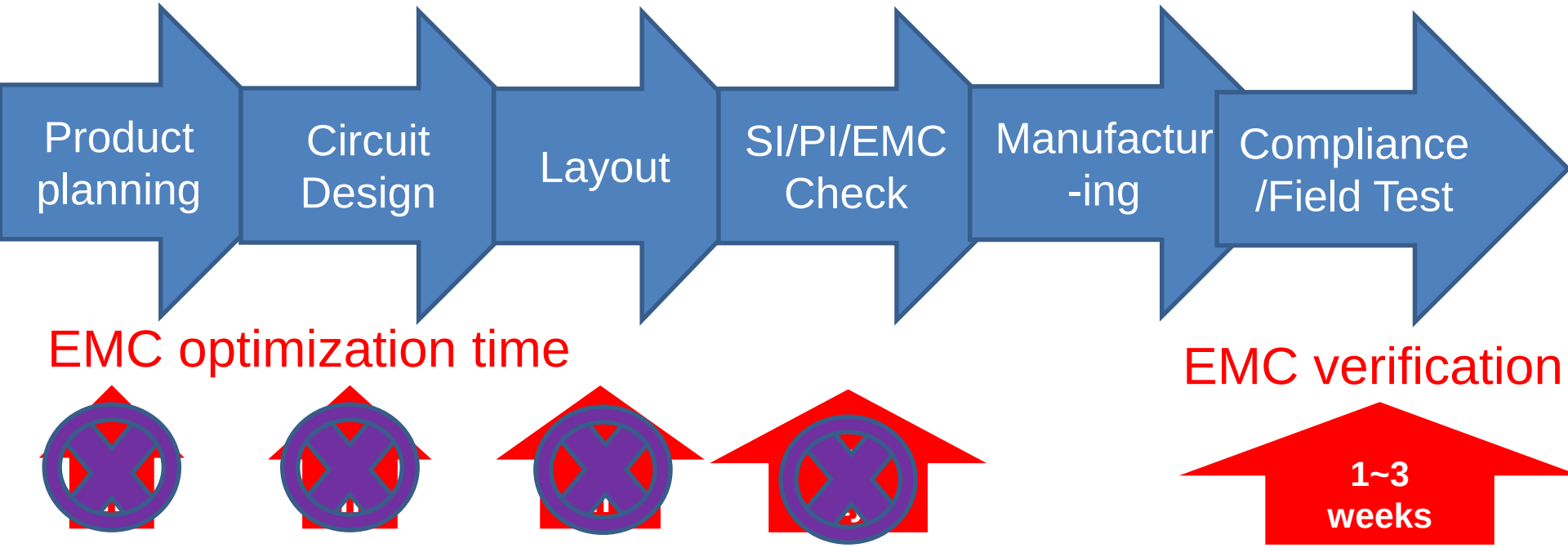
Still …EMC simulation cannot be done at early stage.

What LPB is trying to achieved?



Reach to the target!

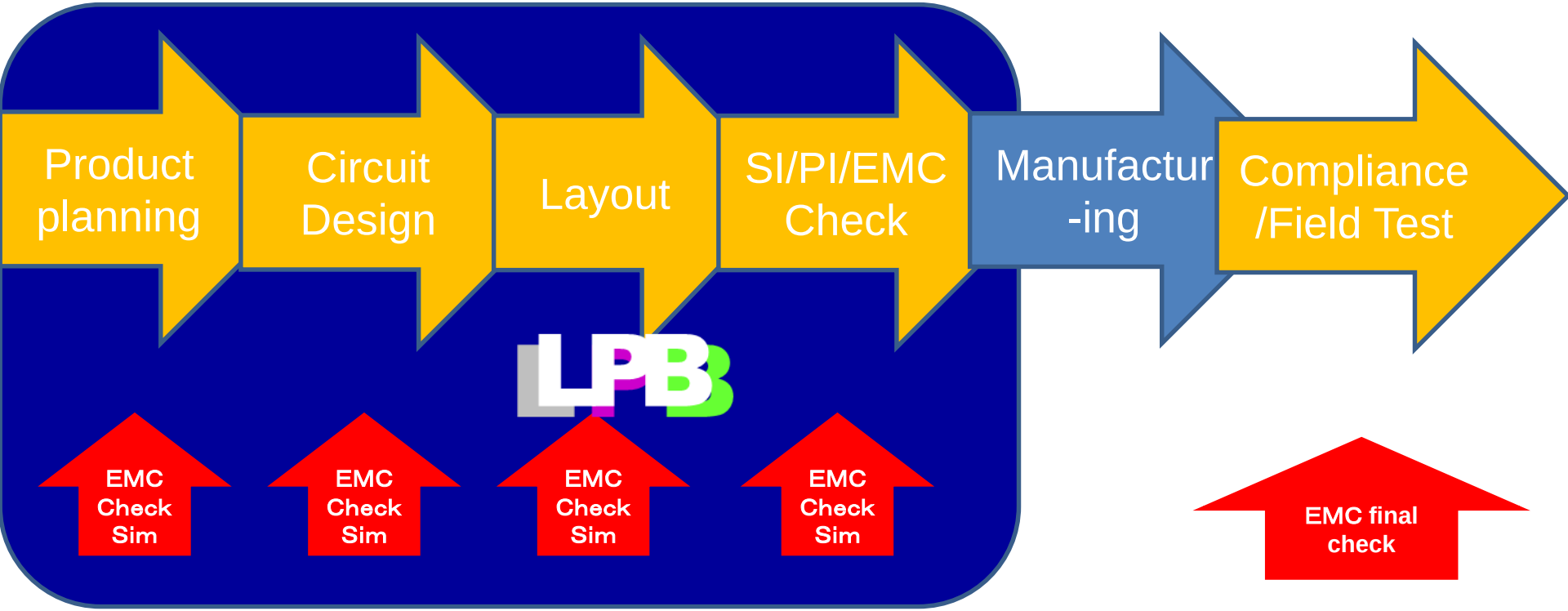
- Finally!



EMC simulation can be done from early stage.

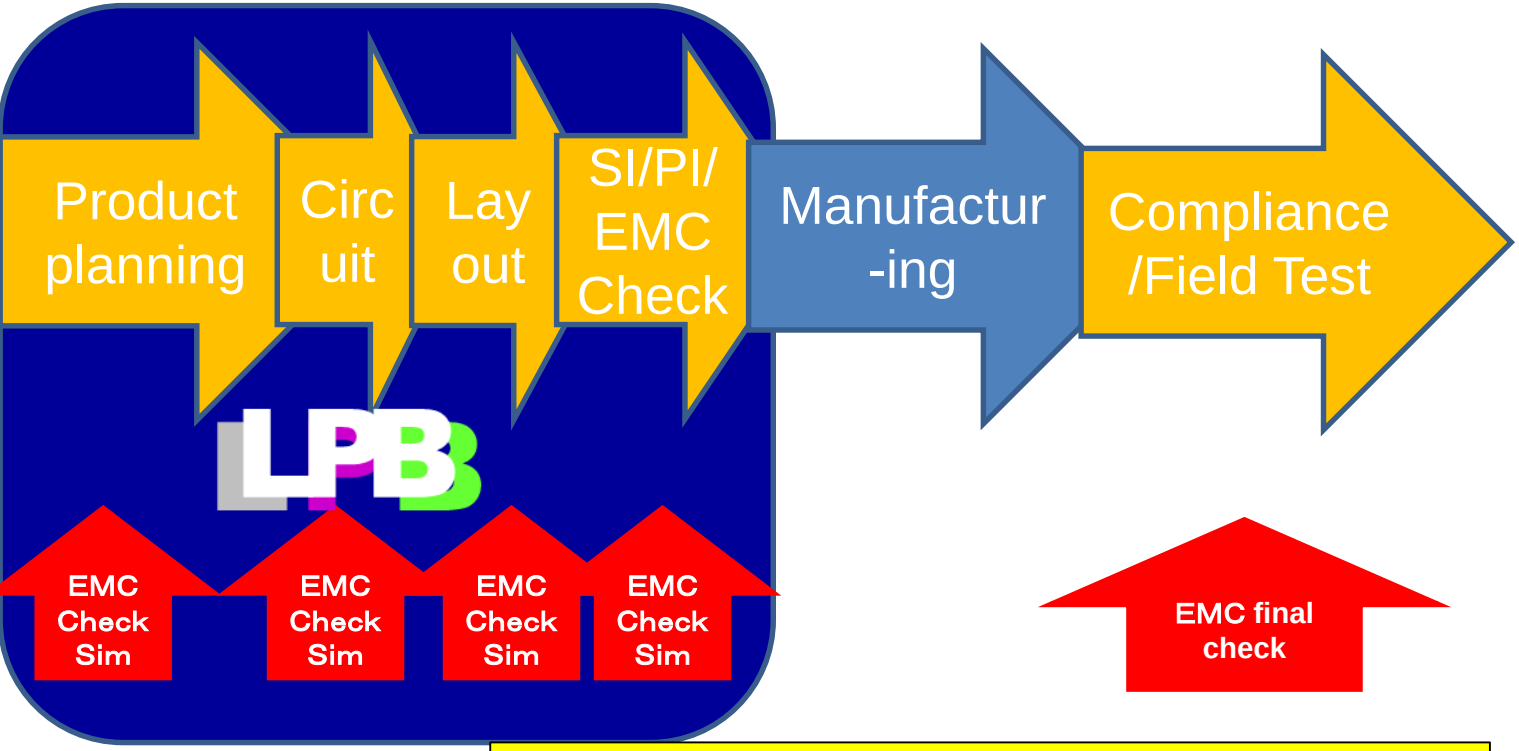
Design and Simulation

- LPB Standard forma is also effective to shorten design process.



Design and Simulation

- LPB Standard forma is also intended to shorten design process.



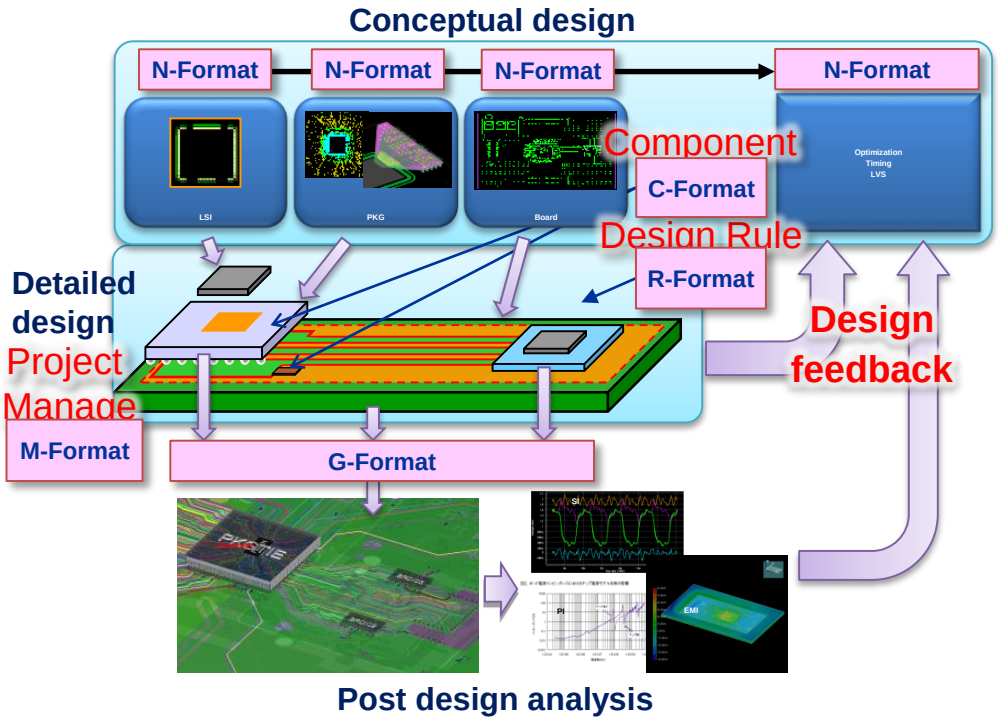
Quality + Time to market

LPB Standard format

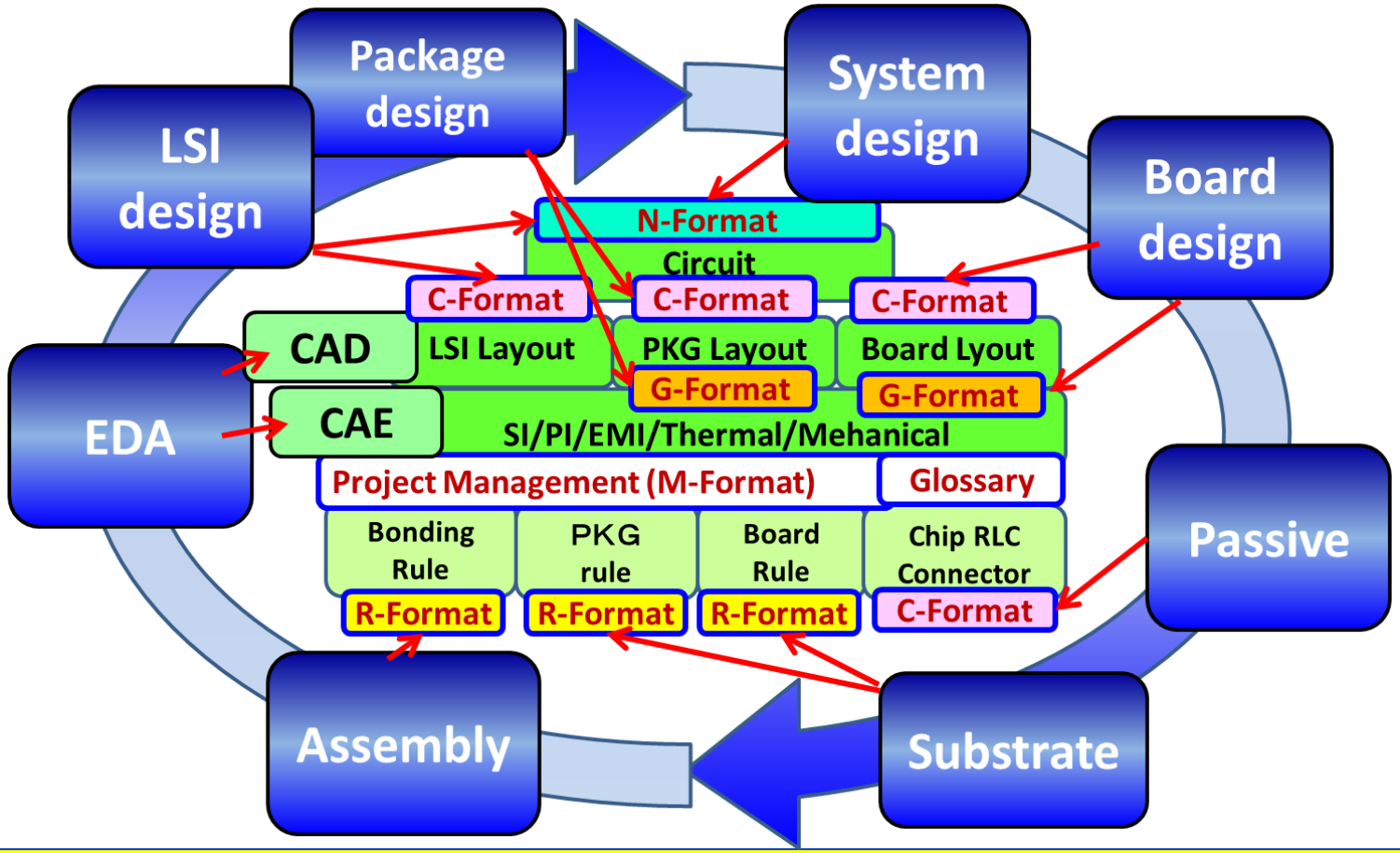
JEITA LPB-WG produce LPB Standard format.

Design environment to be constructed by 6 formats,

1.Project Manage (M-Format)
2.Netlist (N-Format)
3.Component (C-Format)
4.Design Rule (R-Format)
5.Geometry (G-Format)
6.Glossary



Exchange information in supply chain



LPB standard format reveal what the information necessary.
The required information must be shared and are provided in the supply chain.

LPB Community

http://www.lpb-forum.com/

● User/EDA/Suppliers community

LPB Forum

EDA venders
CAD CAE
Develop
LPB interface

Users/Designers
Semiconductor
Electronics products
Implement
LPB design flow

Suppliers
Package, PWB, Passive, Connectors, etc..
Deliver design rule parametric data
With LPB format.

LPB Standard format
is promoted as for **'Forum Standard'.**

Exhibit

Release/Update

Feedback

● Show

edsfair

http://www.edsfair.com/

sponsor

● Standardization committee

LPB JEITA EDA-TC/LPB-WG

9th International Workshop on Electromagnetic Compatibility of Integrated Circuits

EMC Compo 2013

International Standardization Plan

- Standardization Plan

Introduction: DAC2013 2013/6/3-6/5

Submit Project Approval Request(PAR) to IEEE Standard Association @ 2013 Oct.

Approved project: P2401 LPB-WG

Target IEEE standard/IEC dual logo : 2015 June

EDA venders adoption

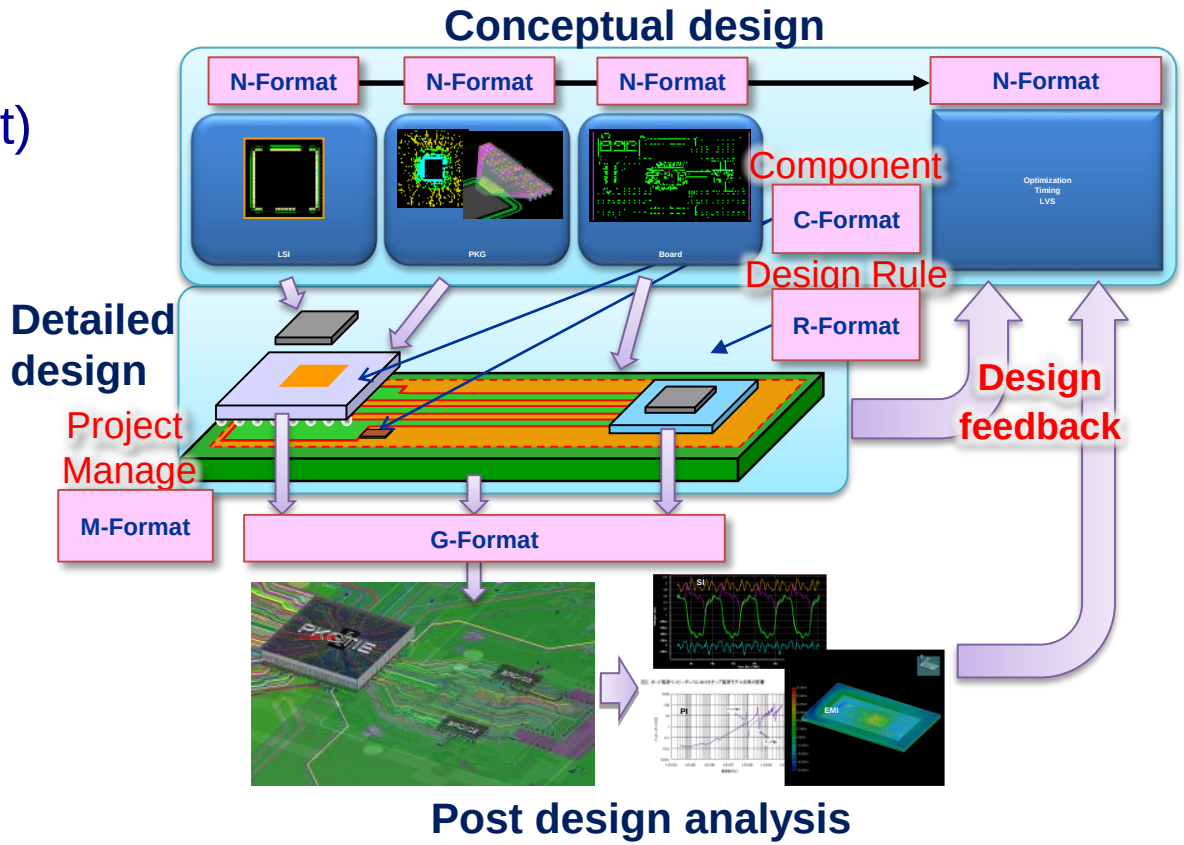
- More then 10 venders already start to develop LPB interface.

LPB Standard Format & Usage example

LPB Standard Format

Design environment to be constructed by 6 formats

1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary



LPB Standard Format Abstract

Format	Abstract	Benefit
Project Management (M-Format)	Manage the LPB files of the LSI, package and board. - Manage the history , revision and update of the files - JEITA original format using XML	Easy to Manage Design history Easy to understand Design Status Understanding The Latest Condition for Verification
Netlist (N-Format)	Connection of the parts - Netlist between LSI, Package and Board. - Verilog HDL format	Easy to Check Connection Between LSI-PKG-Board Enable to Simulate on Board Level
Component (C-Format)	Information of the parts that includes - Pin assignment - Design constraint - Design Status - JEITA original format using XML	Easy to Verify for Optimization of LPB Clarification of Constraint Condition
Design Rule (R-Format)	Rules of the components that includes - Design rule - Assembly rule - Characteristics of the material - JEITA original format using XML	Clarification of Design Rule in Advance Clarification of Verification Condition Easy to Set up for Verification
Geometry (G-Format)	Geometry of the Package and Board - XFL format	Efficient Use of Design Property Use as Reference Design Easy to convert Data

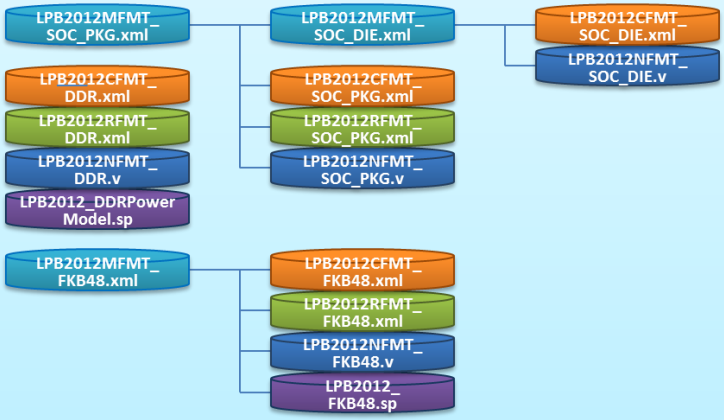
LPB Standard Format Abstract

Project Manage (M-Format)

Abstract

Manage the LPB files of the LSI, package and board.

- Manage the history , revision and update of the files
- JEITA original format using XML



Example

```
<include MFORMAT="MFMT_FKB48.xml" />
<include MFORMAT="MFMT_SOC_PKG.xml" />

<class comment="DDR MEMORY" >
  <CFORMAT   file_name="CFMT_DDR.xml" />
  <RFORMAT   file_name="RFMT_DDR.xml" />
  <NFORMAT   file_name="NFMT_DDR.v" />
  <OtherFile file_name="DDRPowerModel.sp" />
</class>
```

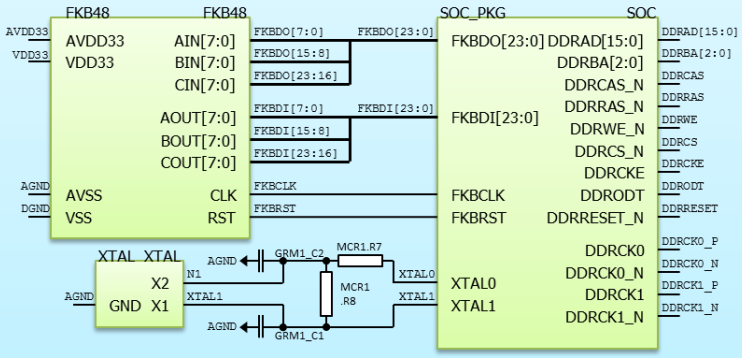
LPB Standard Format Abstract

Netlist (N-Format)

Abstract

Connection of the parts

- Netlist between LSI, Package and Board.
- Verilog HDL format



Example

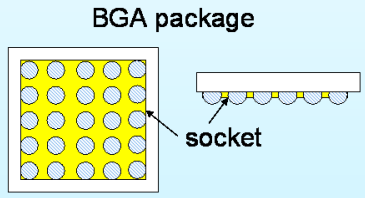
```
module JEITA_SAMPLE ( );
    wire [23:0] FKBDO ;
    wire [23:0] FKBDI ;
    wire VDD33 ; /* PG_NET */
    wire DGND ;  /* PG_NET */

    FKB48 FKB48 ( .AIN(FKBDO),    .AOUT(FKBDI) ) ;
    SOC_PKG SOC ( .FKBDO(FKBDO), .FKBDI(FKBDI) ) ;

endmodule
```

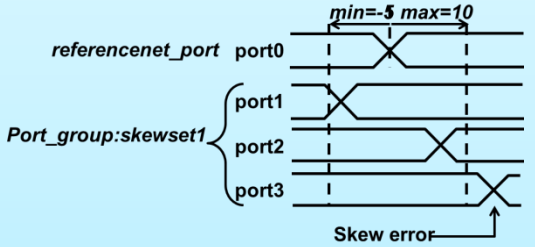
LPB Standard Format Abstract

Component (C-Format)

Abstract

Information of the parts that includes
- Pin assignment
- Design constraint
- Design Status
- JEITA original format using XML





Example

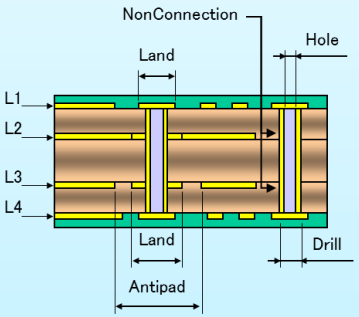
```
<module name="SOC_PKG" type="PKG" shape_id="PKG_BODY" >
  <socket  name="SOC_PKG" >
    <port  id="A5"    x="-8500"   y="12500"   angle="0"  name="FKBDO[5]" />
    <port  id="A6"    x="-7500"   y="12500"   angle="0"  name="FKBDO[2]" />
    <constraint>
      <impedance group_name="FKB_DIN"  type="single" min="40" typ="50" max="60"/>
      <delay     group_name="FKB_DIN"  min="100" typ="150" max="200" />
    </constraint>
  </socket>
</module>
```

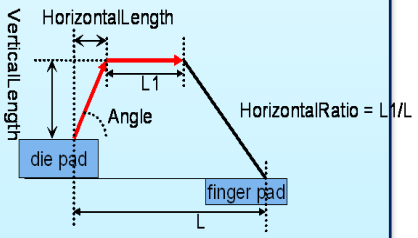
LPB Standard Format Abstract

Design Rule (R-Format)

Abstract

Rules of the components
- Design rule
- Assembly rule
- Characteristics of the material
- JEITA original format using XML



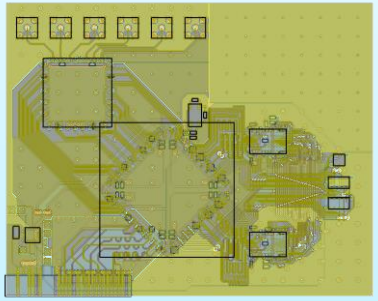


Example

```
<material_def>
  <conductor  material="COPPER" volume_resistivity="1.68e-8" />
  <dielectric material="FR-4"   permittivity="4.5"  tan_delta="0.035" />
</material_def>
<layer_def>
  <layer name="TOP_COND"  type="conductor"  thickness="0.030"
                          conductor_material="COPPER" />
  <layer name="DIELECTRIC12" type="dielectric" thickness="0.100"
                          dielectric_material="FR-4" />
</layer_def>
<spacing_def>
  <layer name="TOP_COND">
    <line_to_line  space="0.050" />
  </layer>
</spacing_def>
```

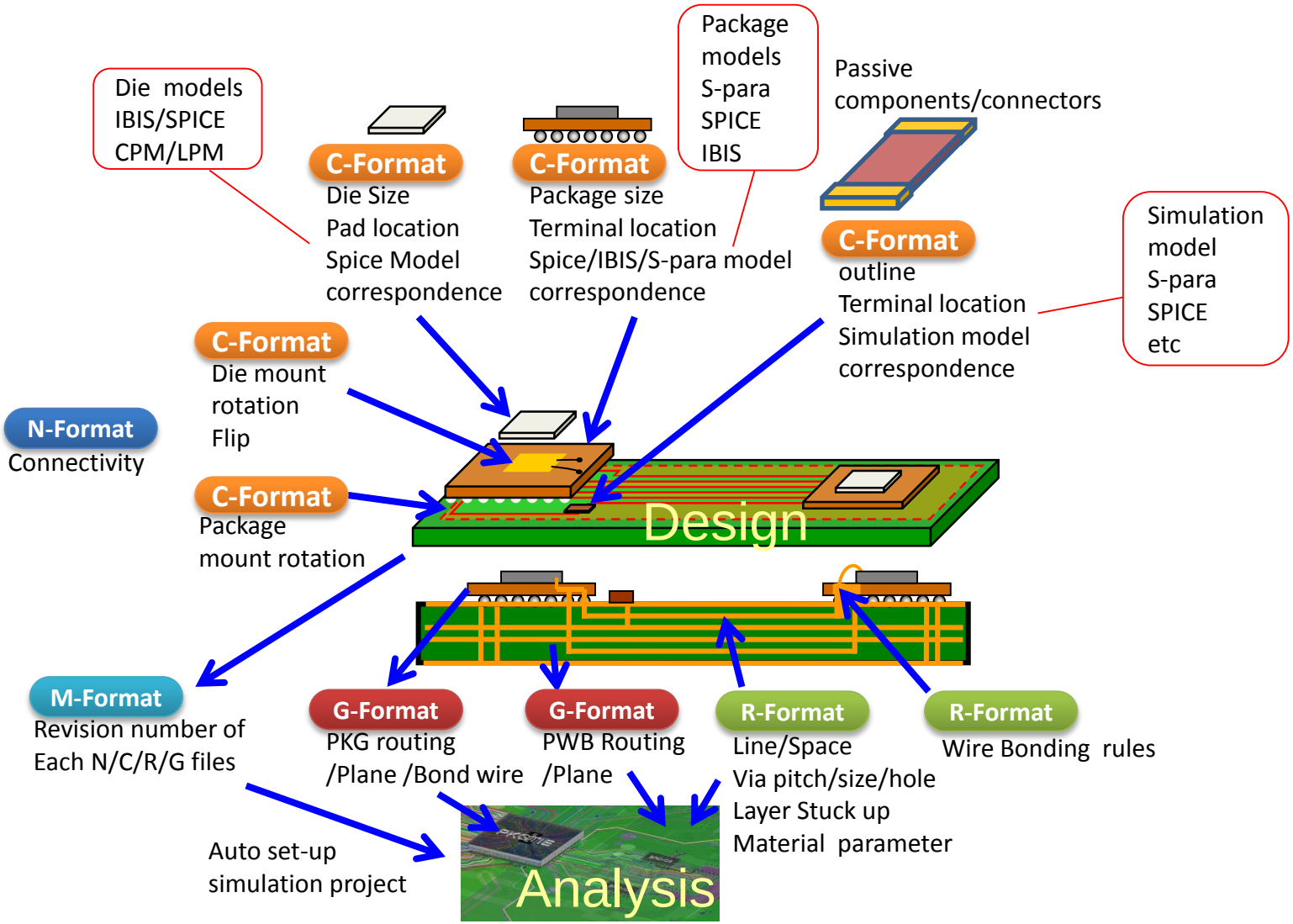
LPB Standard Format Abstract

Geometry (G-Format)

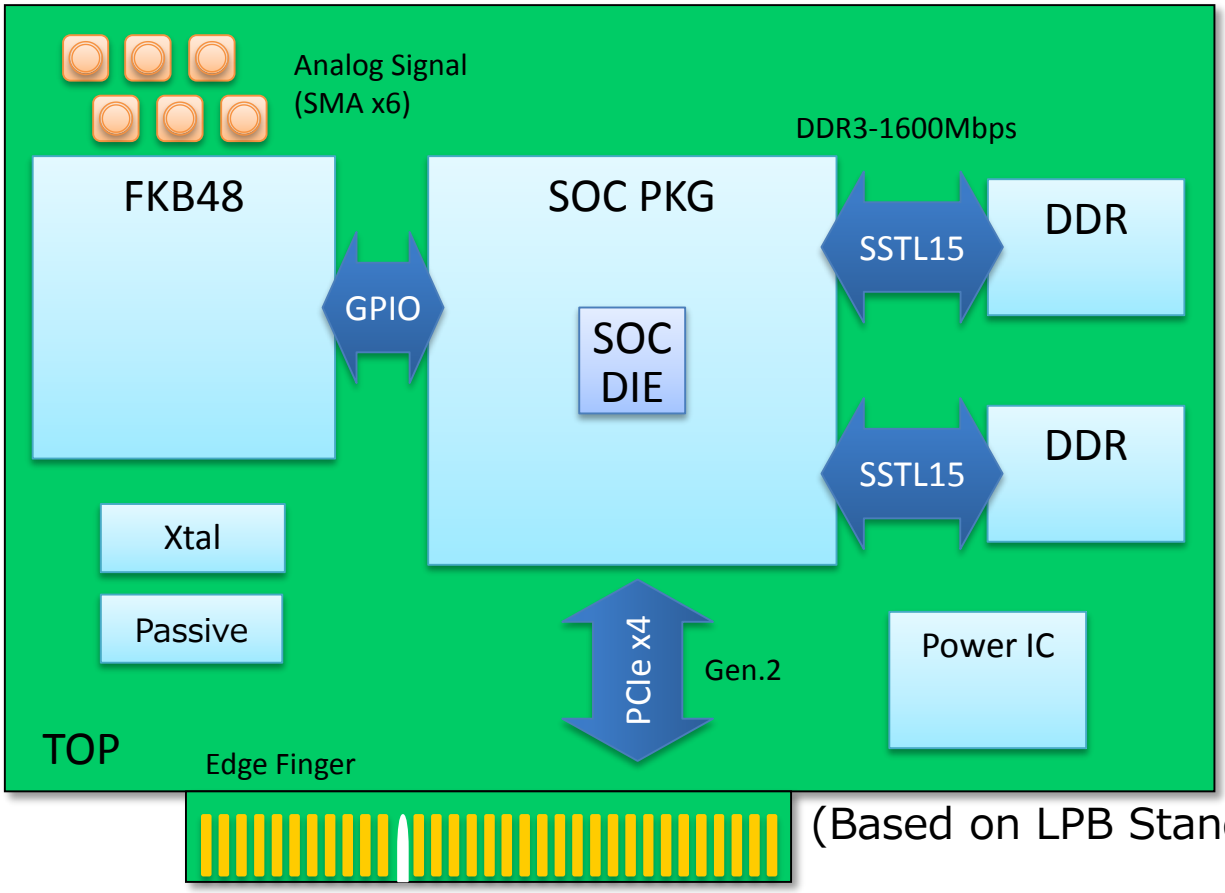
Abstract	Geometry of the Package and Board - XFL format 

Example	`shape 1 4 53.2 26.8 90 N`
	`via 1 4 V020C060C085 54.55 20 0 N`
	`via 2 3 B010C050C075C23 41 24.25 0 N`
	`shape 1 11 35.5 29 0 N`
	`via 1 2 B010C030C12 35.5 29 0 N`
	`path 2 0.1 {`
	`  41 24.25`
	`  41.000000 24.750000`
	`}`

LPB Files Delivery



LPB sample files for test bench

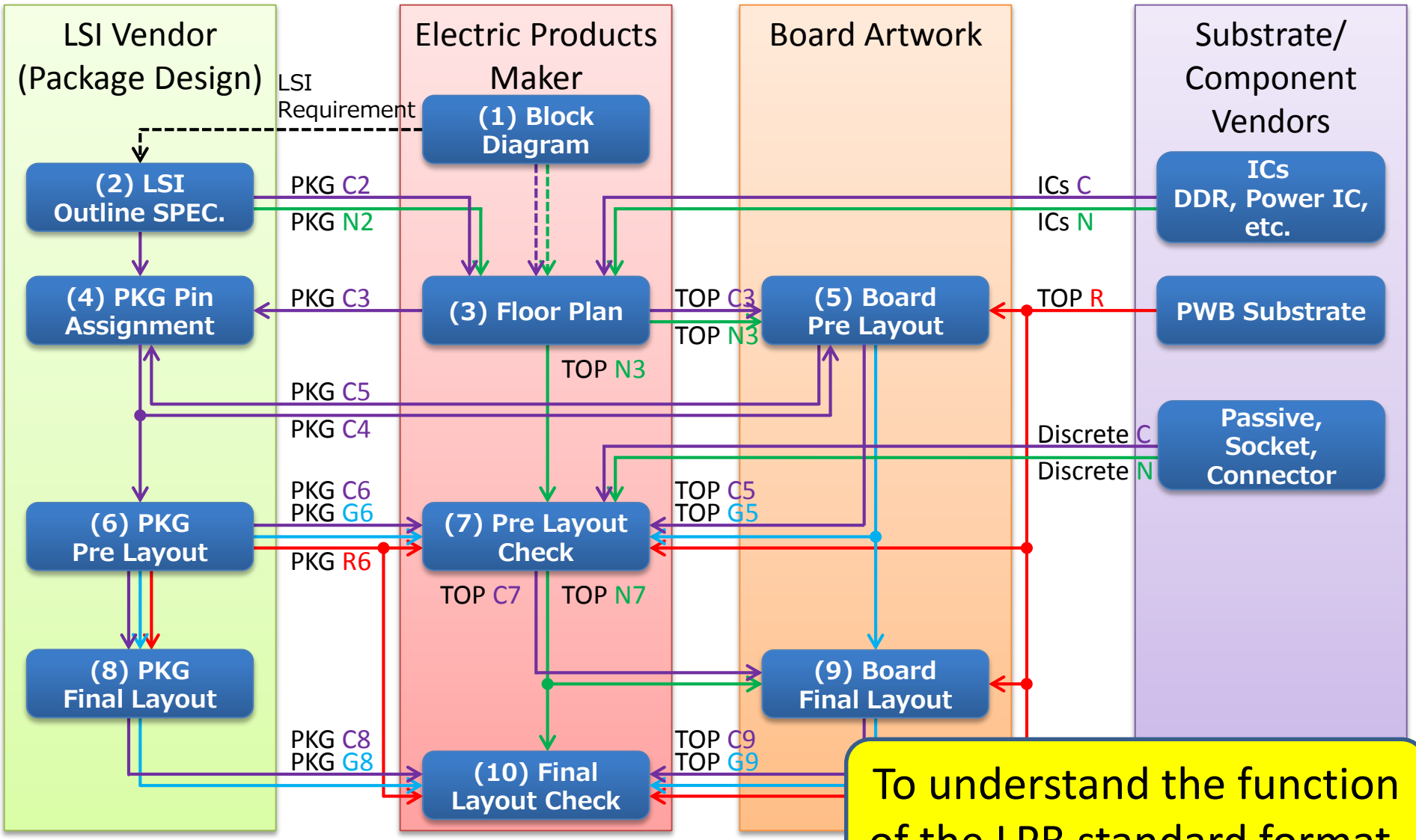


Component	Details
SOC	New Design
DDR	generic parts
FKB48	generic parts
Power IC	generic parts
Xtal	generic parts
Passive	generic parts

(Based on LPB Standard Format Ver.2.1)

Golden Sample are provided as a test bench for implementation.

Reference flow using LPB standard format



To understand the function of the LPB standard format.

Growth of LPB files in design steps

C-Format

Header	header	Header
Global	unit	Defines the unit
	shape	Defines the shape
	pad sta	ack
Module	socket	output ports of the module
	port	Defines the port shape, name and locaion
	port group	
	power domain group	power domain of the signals
	swappable port/group	Defines the swappable ports/port groups
	frequency	frequency for the port
	constraint	upper hierarchy
	specification	Defines the specification of the module
	reference	Defines the connection procedure between ports in socket section and ports in referenced file.
Component	placement	Defines the placement of the module

LPB files will grow every time you go through the process of the design.

Port ID, Coordinate, Port Name

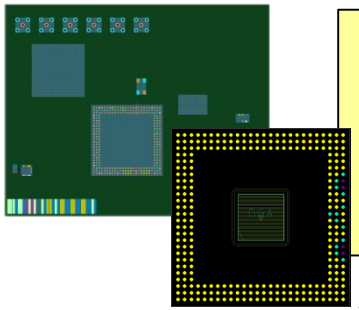
Swappable Ports/Port groups

Impedance, Delay, Skew

Placement Information of the parts

```
[Example]
 <placement ref_module="SOC" inst="SOC"  x="400"   y="-6500" />
 <placement ref_module="DDR" inst="DDR0" x="37000" y="-3200" />
```

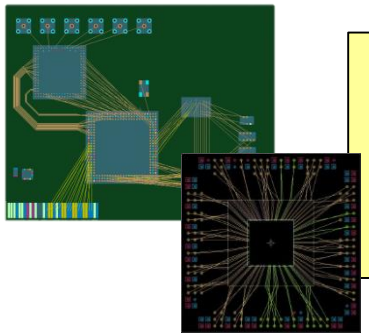
<Example> The growth of C-format



```
<port id="A3"  x="-10500"  y="12500"  angle="0" />
<port id="A4"  x="-9500"   y="12500"  angle="0" />
<port id="A5"  x="-8500"   y="12500"  angle="0" />
<port id="A6"  x="-7500"   y="12500"  angle="0" />
<port id="A7"  x="-6500"   y="12500"  angle="0" />
<port id="A8"  x="-5500"   y="12500"  angle="0" />
<port id="A9"  x="-4500"   y="12500"  angle="0" />
```

Coordinate of port only

PKG-C2

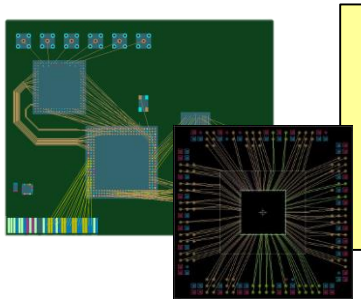


```
<port id="A3"  x="-10500"  y="12500"  angle="0" />
<port id="A4"  x="-9500"   y="12500"  angle="0" />
<port id="A5"  x="-8500"   y="12500"  angle="0"  name="FKBDO[3]"  direction="out"   type="signal" />
<port id="A6"  x="-7500"   y="12500"  angle="0"  name="FKBDO[0]"  direction="out"   type="signal" />
<port id="A7"  x="-6500"   y="12500"  angle="0" />
<port id="A8"  x="-5500"   y="12500"  angle="0" />
<port id="A9"  x="-4500"   y="12500"  angle="0"  name="XTAL1"     direction="inout"  type="signal" />
```

Add Name of the port by Board designer

PKG-C3

Dispute?



```
<port id="A3"  x="-10500"  y="12500"  angle="0" />
<port id="A4"  x="-9500"   y="12500"  angle="0" />
<port id="A5"  x="-8500"   y="12500"  angle="0"  name="FKBDO[5]"  direction="out"   type="signal" />
<port id="A6"  x="-7500"   y="12500"  angle="0"  name="FKBDO[2]"  direction="out"   type="signal" />
<port id="A7"  x="-6500"   y="12500"  angle="0" />
<port id="A8"  x="-5500"   y="12500"  angle="0"  name="VDD_PLL"   direction="inout"  type="power" />
<port id="A9"  x="-4500"   y="12500"  angle="0"  name="XTAL1"     direction="inout"  type="signal" />
```

Change the assignment by Package designer

PKG-C4

LPB files grow and share the information each other.

<Example> The growth of C-format

PKG-C3

```
<!-- Swappable Group -->

<!-- Swappable Port -->
```

No info. about port swap

PKG-C4

```
<!-- Swappable Group -->
    <swappable_group>
       <ref_portgroup name="FKB_DIN_BYTE0" />
       <ref_portgroup name="FKB_DIN_BYTE1" />
       <ref_portgroup name="FKB_DIN_BYTE2" />
    </swappable_group>

<!-- Swappable Port -->
    <swappable_port>
       <ref_port name="FKBDO[0]" />
       <ref_port name="FKBDO[1]" />
       <ref_port name="FKBDO[2]" />
       <ref_port name="FKBDO[3]" />
       <ref_port name="FKBDO[4]" />
       <ref_port name="FKBDO[5]" />
       <ref_port name="FKBDO[6]" />
       <ref_port name="FKBDO[7]" />
    </swappable_port>
```

Her is additional preparation

Add swappable info.

Give the constraint from package designer to board designer

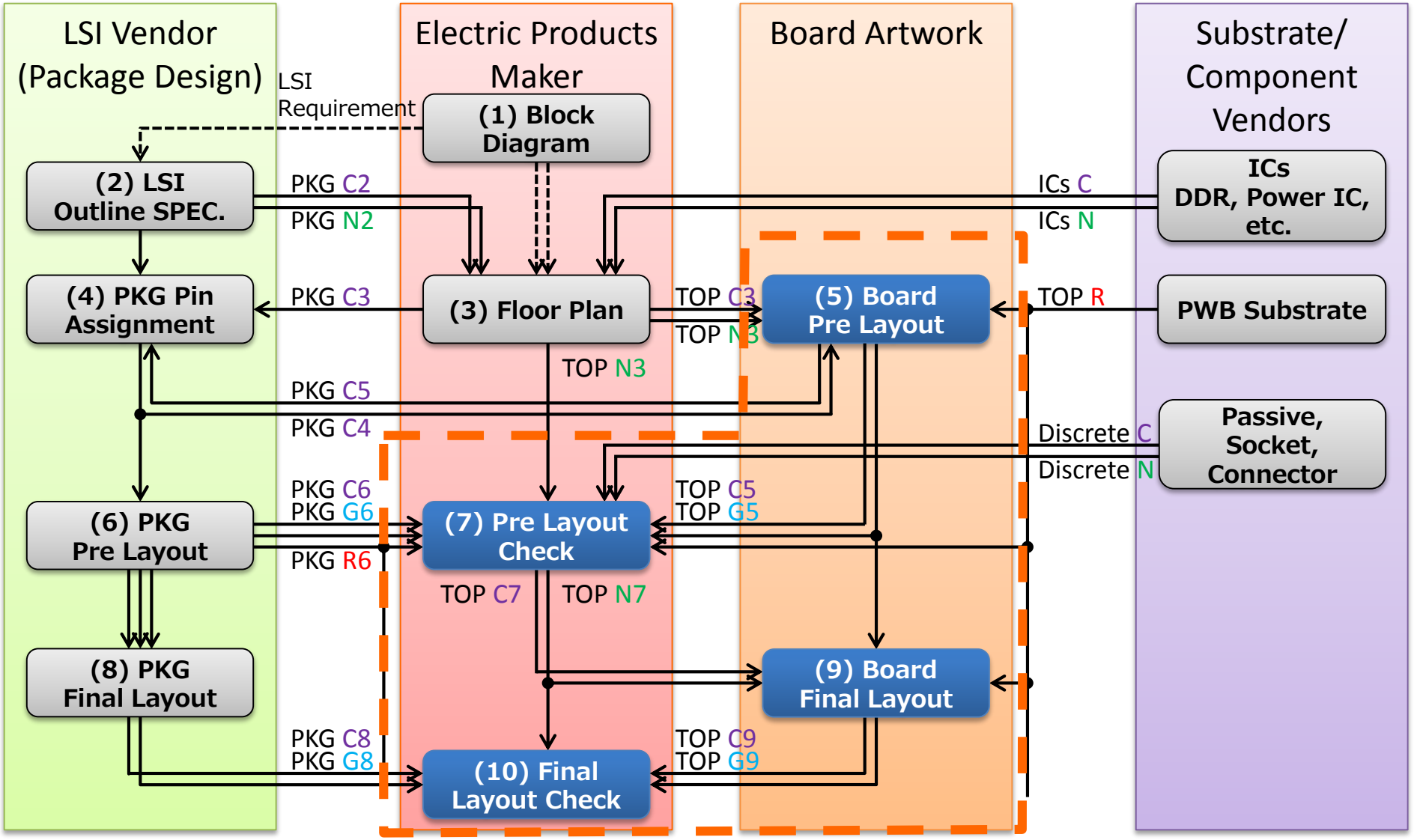
Based on the constraint, board designer can change the design

Share the information about constraint and flexibility

=> change of design proposal is possible

Reference Flow
Demonstration

Reference flow using LPB standard format

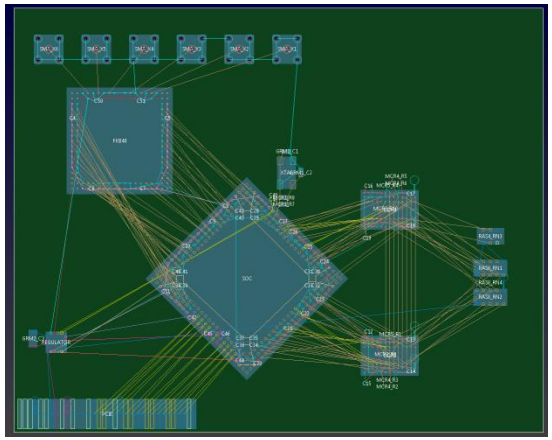


(5) Board Pre Layout

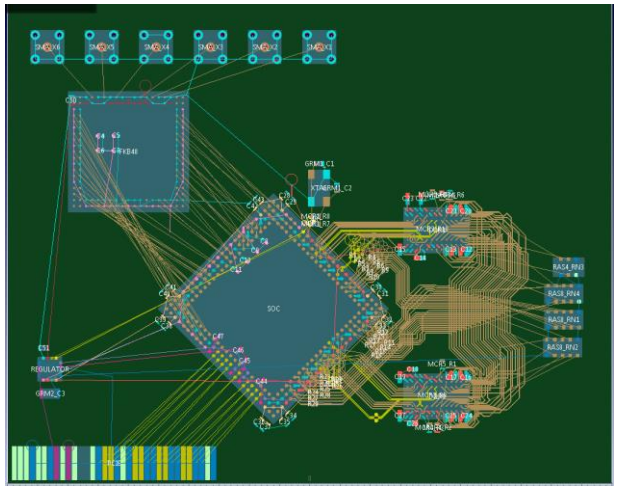
Design Force CR-8000

LPB format

Floorplan Result.
Tentative pin assignment is done.



Optimize Placement



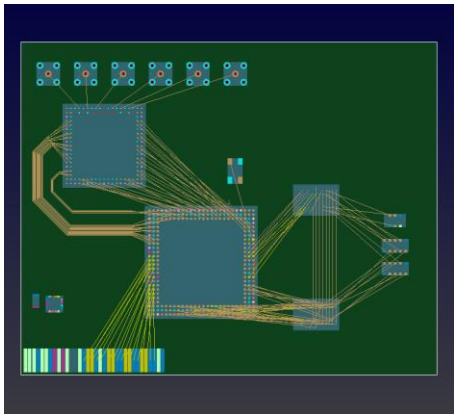
Critical Path Routing

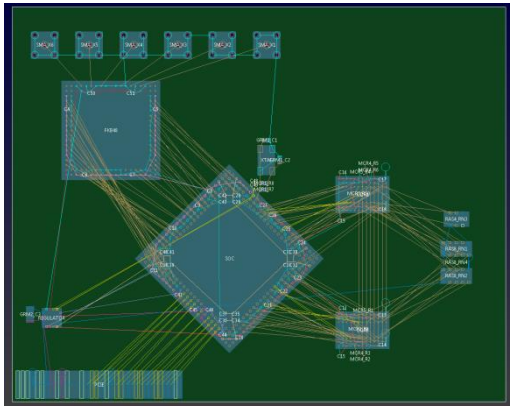
LPB format

Add the change of floorplan and pin assignment.

(5) Board Pre Layout

Change placement info.





```
<placement y="-8223.2" x="30206.5" mount="TOP" angle="270" z="200" inst="DDR0" ref_module="DDR"/>
<placement y="15911.7" x="36947.6" mount="TOP" angle="270" z="200" inst="DDR1" ref_module="DDR"/>
<placement y="-6500" x="400" mount="TOP" angle="0" z="200" inst="SOC" ref_module="SOC_PKG"/>
<placement y="22417.2" x="-8150.9" mount="TOP" z="20" inst="GRM1_C1" ref_module="GRM1"/>
<placement y="23603.4" x="-4479.3" mount="TOP" z="20" inst="GRM1_C2" ref_module="GRM1"/>
```

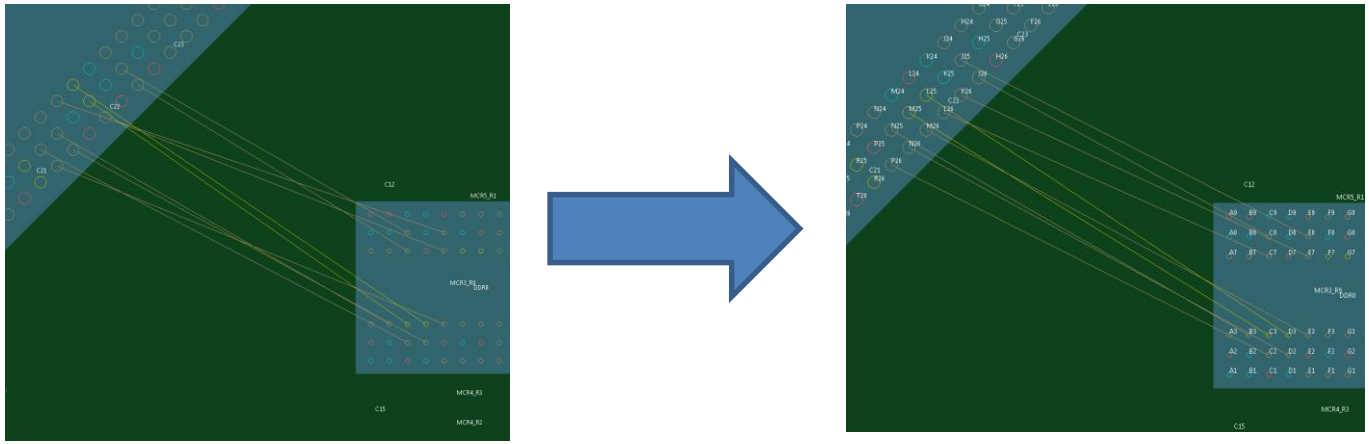
TOP C3

TOP C5

```
<placement y="-3223.2" x="37206.5" mount="TOP" angle="90" z="200" inst="DDR0" ref_module="DDR"/>
<placement y="10911.7" x="30947.6" mount="TOP" angle="90" z="200" inst="DDR1" ref_module="DDR"/>
<placement y="-6500" x="400" mount="TOP" angle="45" z="200" inst="SOC" ref_module="SOC_PKG"/>
<placement y="22417.2" x="-8150.9" mount="BOTTOM" z="20" inst="GRM1_C1" ref_module="GRM1"/>
<placement y="23603.4" x="-4479.3" mount=" BOTTOM " z="20" inst="GRM1_C2" ref_module="GRM1"/>
```

(5) Board Pre Layout

Swap pin



```
<port id="R24" type="signal" y="-1500" x="10500" name="DDRDQ[0]" direction="inout"/>
<port id="R25" type="signal" y="-1500" x="11500" name="DDRDQ[1]" direction="inout"/>
<port id="R26" type="signal" y="-1500" x="12500" name="DDRDQ[2]" direction="inout"/>
<port id="P24" type="signal" y="  -500" x="10500" name="DDRDQ[3]" direction="inout"/>
<port id="P25" type="signal" y="  -500" x="11500" name="DDRDQ[4]" direction="inout"/>
<port id="P26" type="signal" y="  -500" x="12500" name="DDRDQ[5]" direction="inout"/>
```

PKG C4

```
<port id="R24" type="signal" y="-1500" x="10500" name="DDRDQ[7]" direction="inout"/>
<port id="R25" type="signal" y="-1500" x="11500" name="DDRDQ[0]" direction="inout"/>
<port id="R26" type="signal" y="-1500" x="12500" name="DDRDQ[2]" direction="inout"/>
<port id="P24" type="signal" y="  -500" x="10500" name="DDRDQ[6]" direction="inout"/>
<port id="P25" type="signal" y="  -500" x="11500" name="DDRDQ[3]" direction="inout"/>
<port id="P26" type="signal" y="  -500" x="12500" name="DDRDQ[4]" direction="inout"/>
```

PKG C5

Simulation Setup

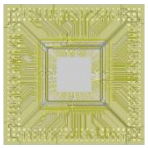
Input for Simulation :

Layout Tools :

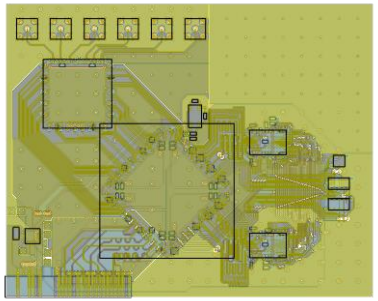
- Zuken　Design Force
- Cadence　APD
- etc…

- Board, Package Geometry
  - Traces, Vias, Pads
  - Planes, Polygons
  - etc…

G-Format



Package
Designed by APD



Board
Designed by Design Force

Extraction Tools :

- ANSYS　ANSYS SIwave, ANSYS HFSS
- etc…

Simulation Setup

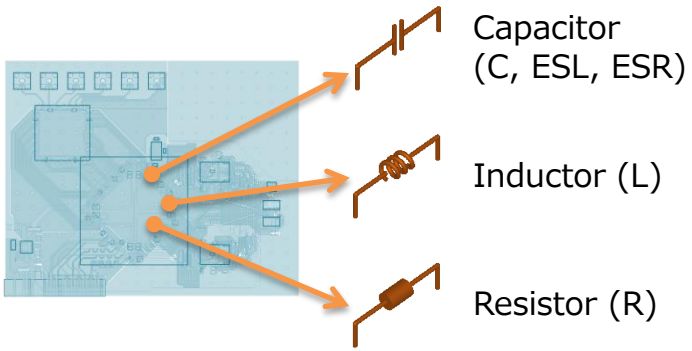
Input for Simulation :

Layout Tools :

- Zuken　Design Force
- Cadence　APD
- etc…

- Passive Components
  - C, L, R
- Constraints
  - Skew, Frequency, etc…

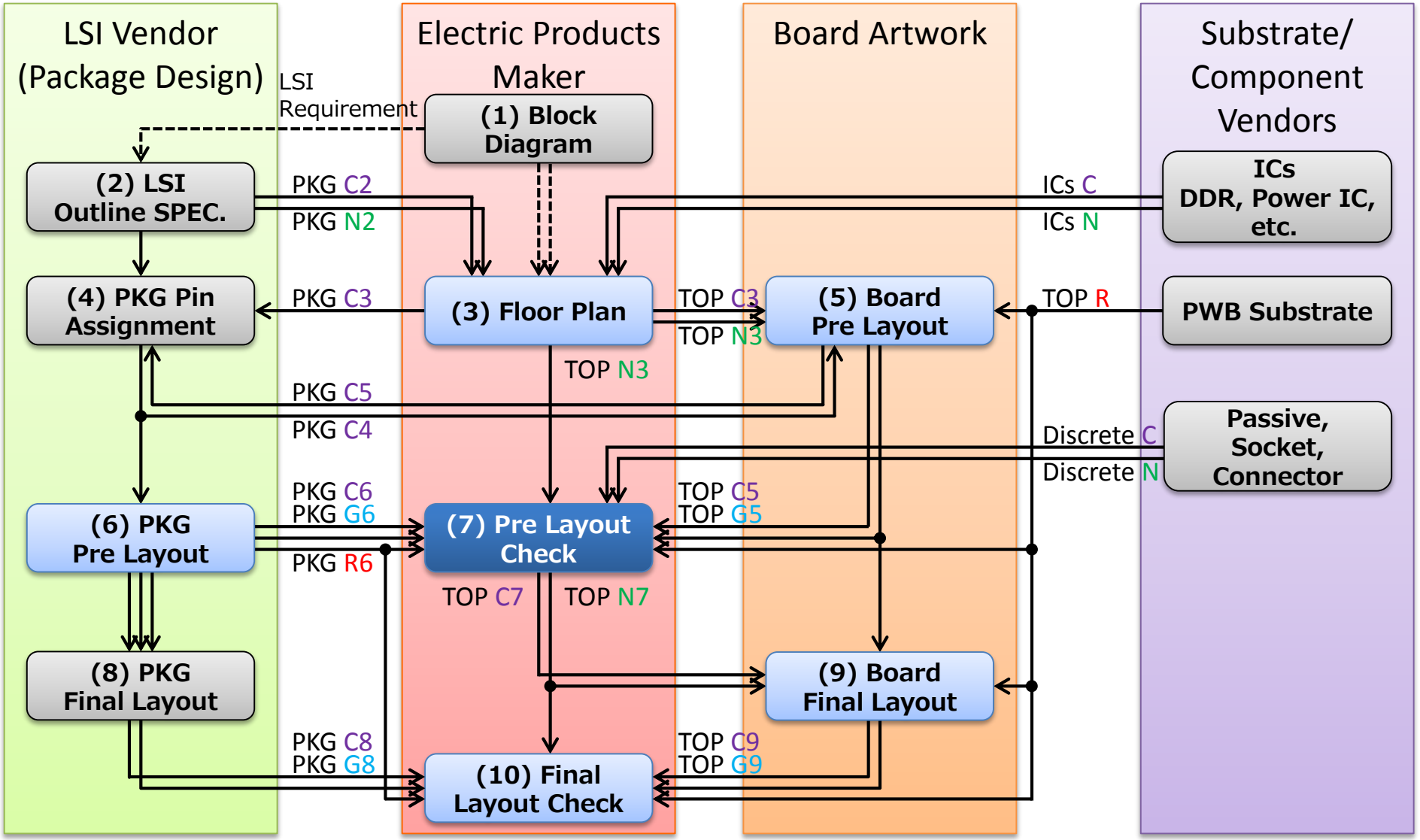
C-Format



Extraction Tools :

- ANSYS　ANSYS SIwave, ANSYS HFSS
- etc…

(7) Pre Layout Check



(7) Pre Layout Check

Works :

(7) Pre Layout Check

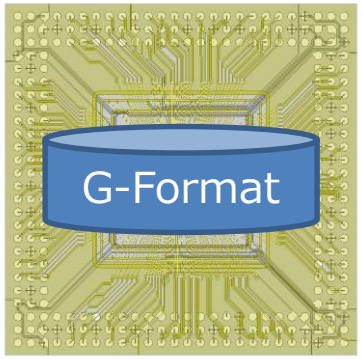
【Signal Integrity Simulation of Critical Nets】

- Timing Verification of DDRIII 1.3GBps Write Cycle
  - ✓ Is Damping Resistors required?
  - ✓ What is the best ODT setting?
  - ✓ Estimate the worst skew of DQ

(7) Pre Layout Check

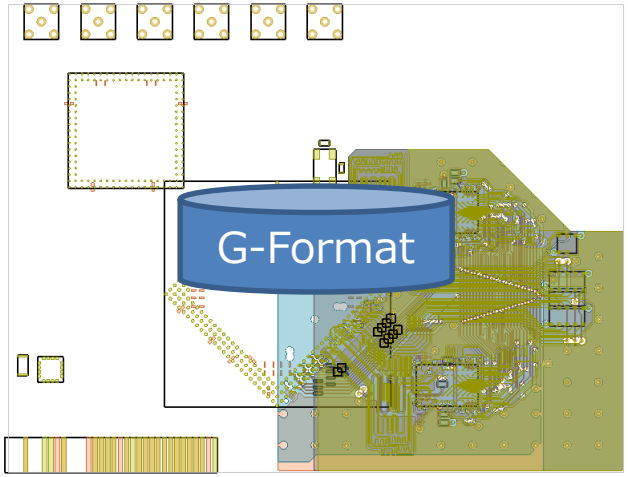
Geometry :

【Package】



- Designed by Cadence APD
- All nets are completely routed
- DQs are NOT isometric

【Board】



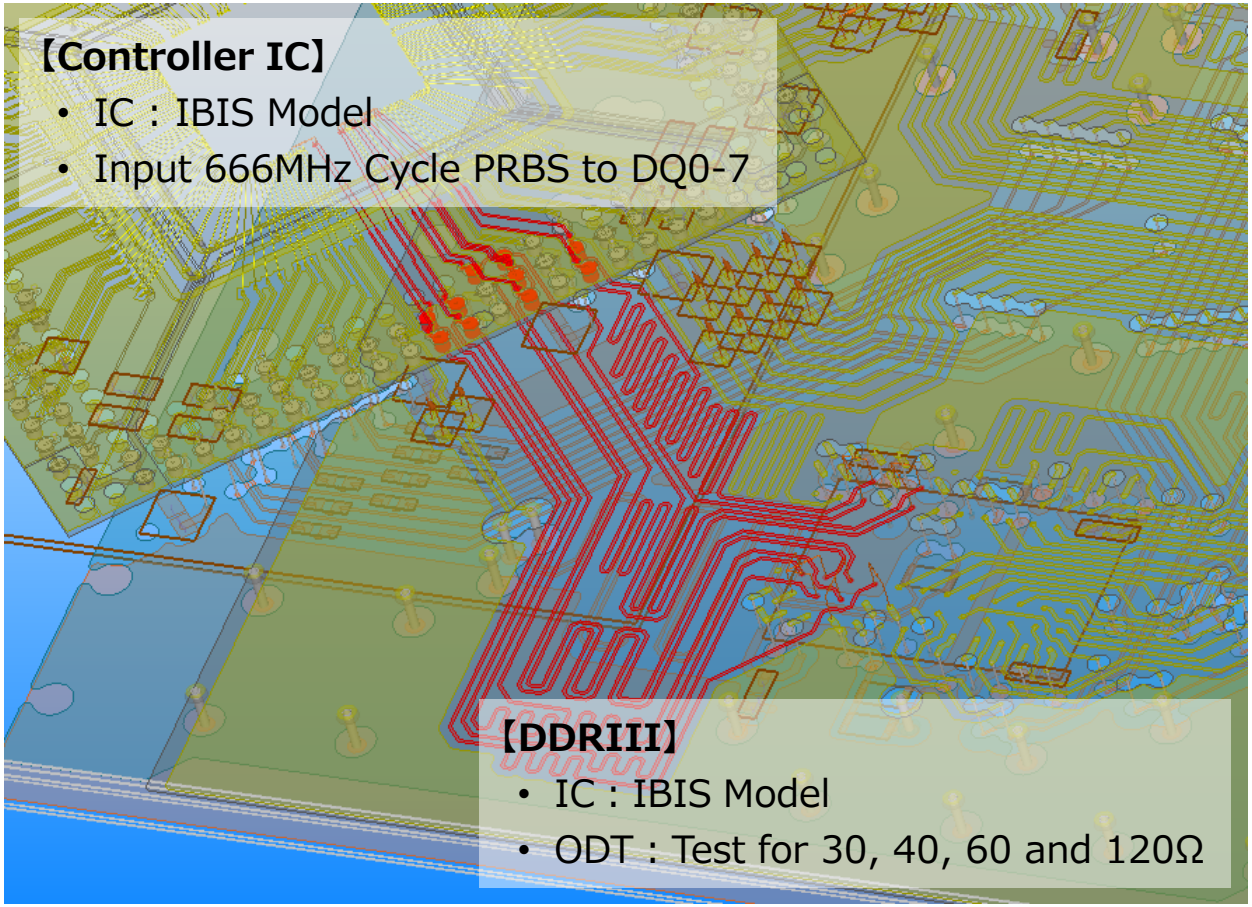
- Designed by Zuken Design Force
- Only 1.5V Power, Ground, DQS and DQ
- DQS and DQs are isometric

ANSYS SIwave

Merged and stacked in Extraction Tool

(7) Pre Layout Check

Overview of Simulation :



DQS, DQ signals in Package and Board Layout / ANSYS SIwave (Extraction Tool)

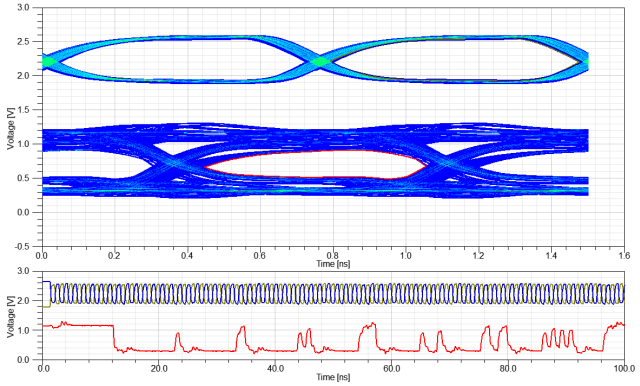
(7) Pre Layout Check

Simulation Result :

Eye Diagram (ODT : 30Ω (FAIL))

DQS

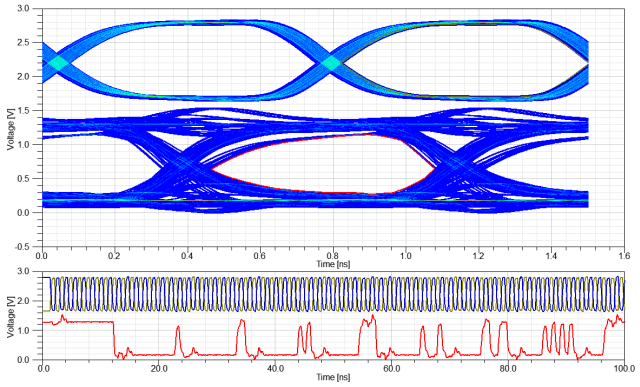
DQ0



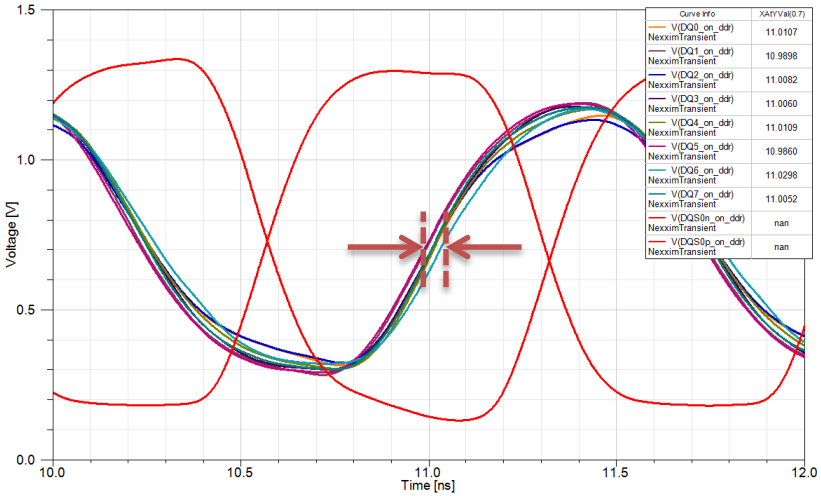
Eye Diagram (ODT : 60Ω (Best Case))

DQS

DQ0



Transient Waveform of DQS and DQ0～7



【Worst Skew (Case of ODT=60Ω)】

- 42.8ps (DQ5-DQ6)

Eye Diagram and Transient Waveform / ANSYS DesignerSI (Circuit Simulator)

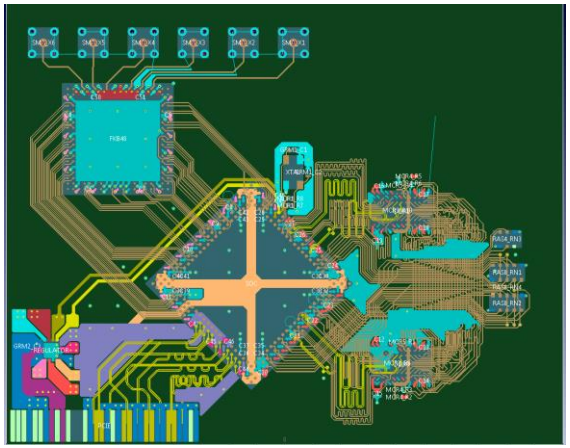
(9) Board Final Layout

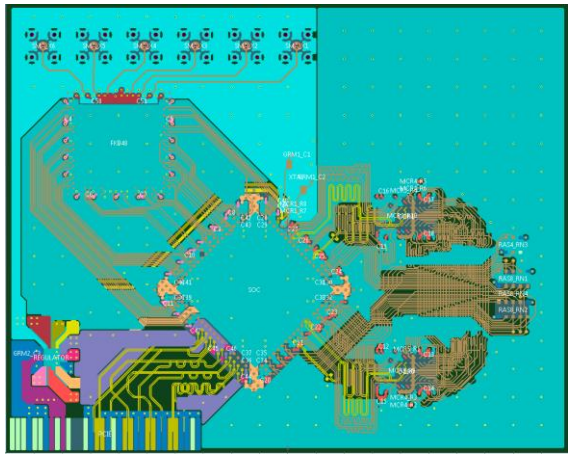
Import the result of pre layout check
- Skew
- Decap

LPB format

Re design to satisfy the constraints.
- Change pin assignment
- Change decap

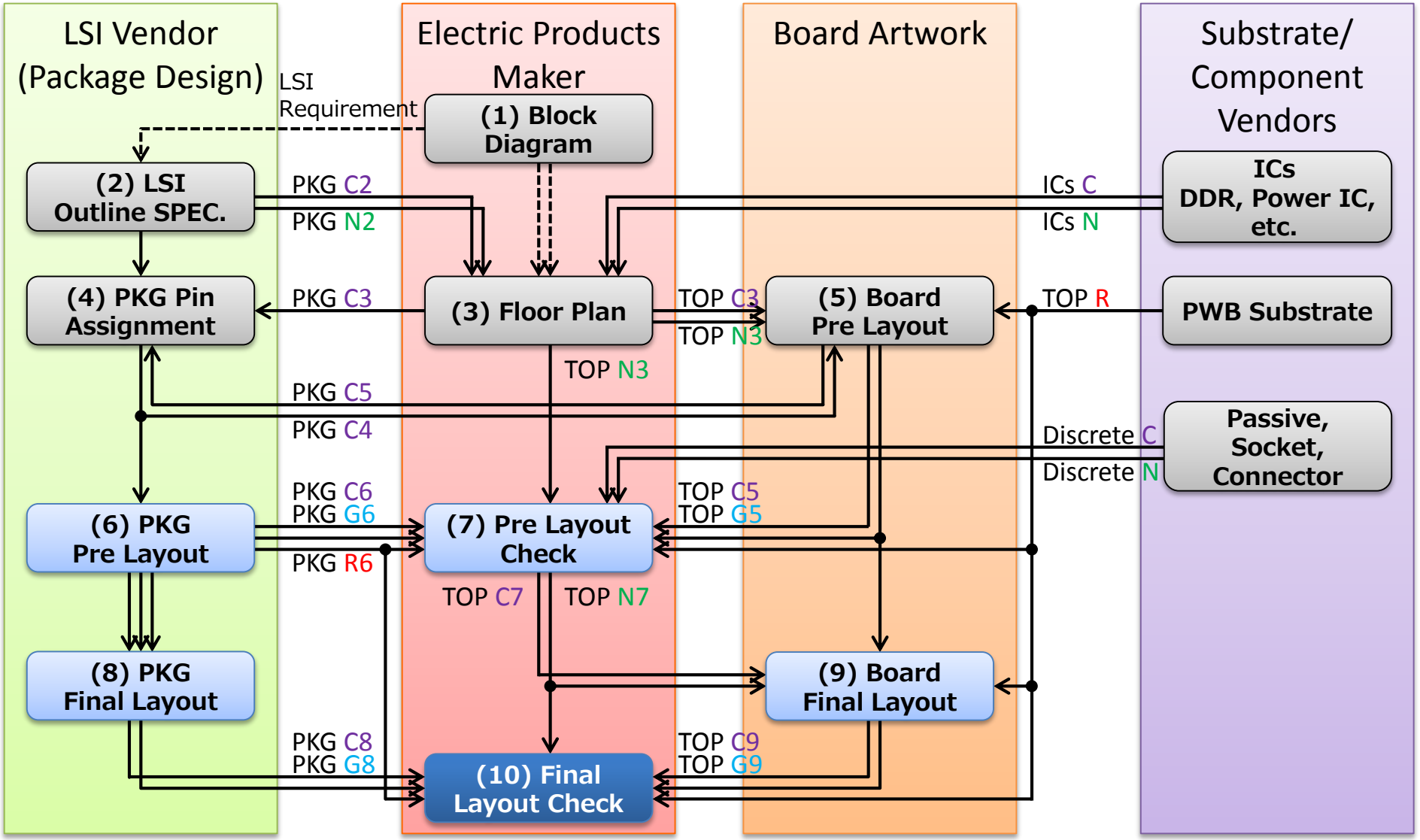
Route other signal
Design power/ground





Design Force CR-8000

(10) Final Layout Check



(10) Final Layout Check

Works :

(10) Final Layout Check

【Power Integrity Simulation of PDN】

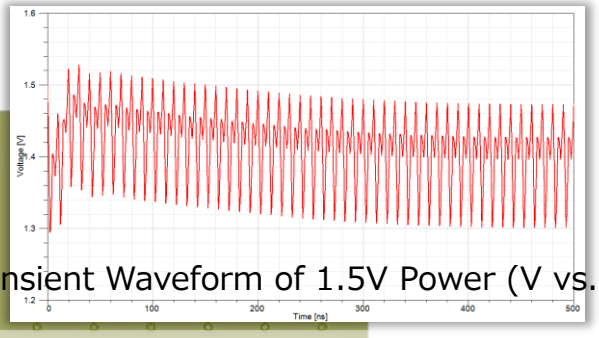
- Input Impedance Analysis of Controller IC and Bypass Caps Optimization
  - ✓ Chip-Package-System Total Impedance
  - ✓ Bypass Caps Optimization

【EMI (Far/Near Field) Simulation】

- Far/Near Field analysis induced by Power Noise
  - ✓ CISPR 22 Test (Far Field)
  - ✓ Checks Near Field

(10) Final Layout Check

Overview of Simulation :



Transient Waveform of 1.5V Power (V vs. T)

【Controller IC】
- IC : CPM (Chip Power Model / Apache RedHawk)
- Place Port between 1.5V Power and Ground

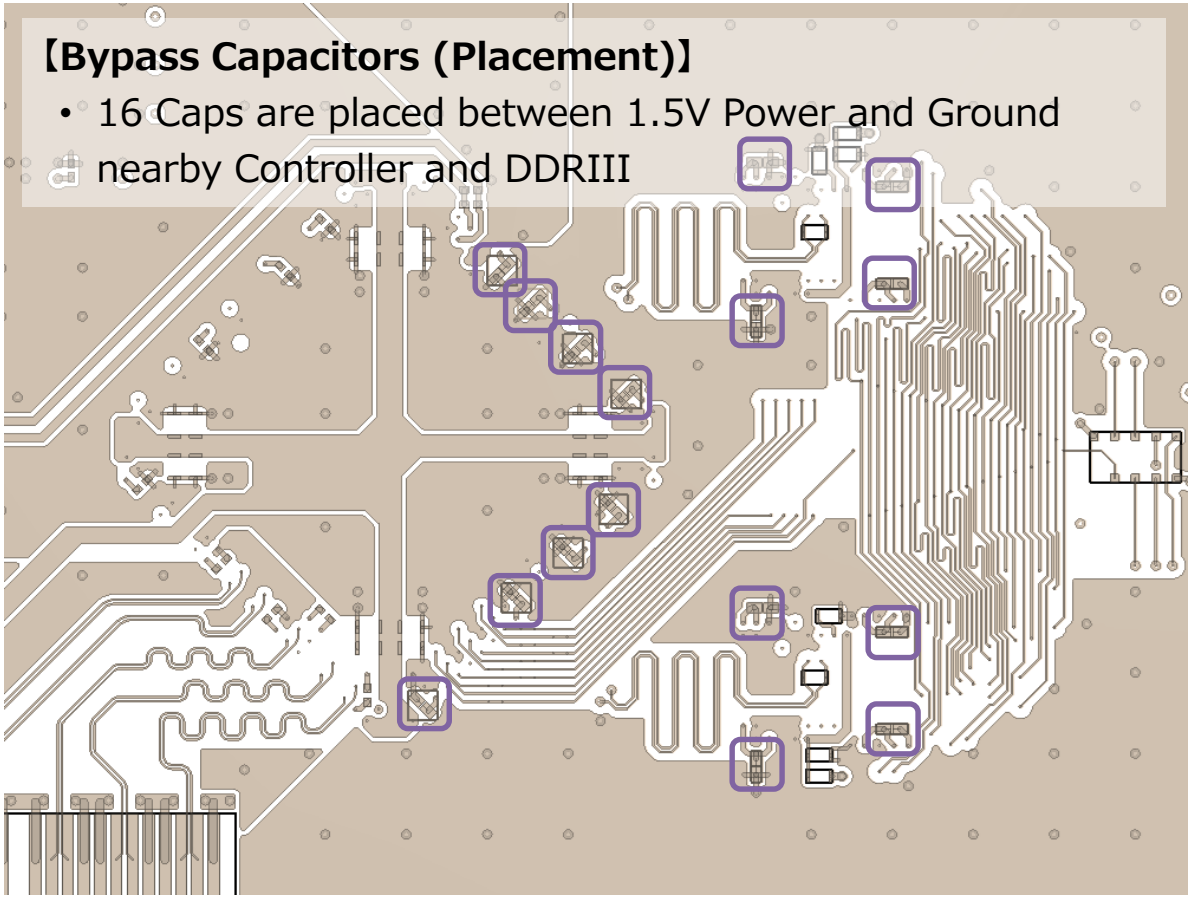
【Regulator】
- DC 1.5V Power Supply

【Bypass Capacitors】
- 16 Caps for 1.5V Power

Package and Board Layout / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

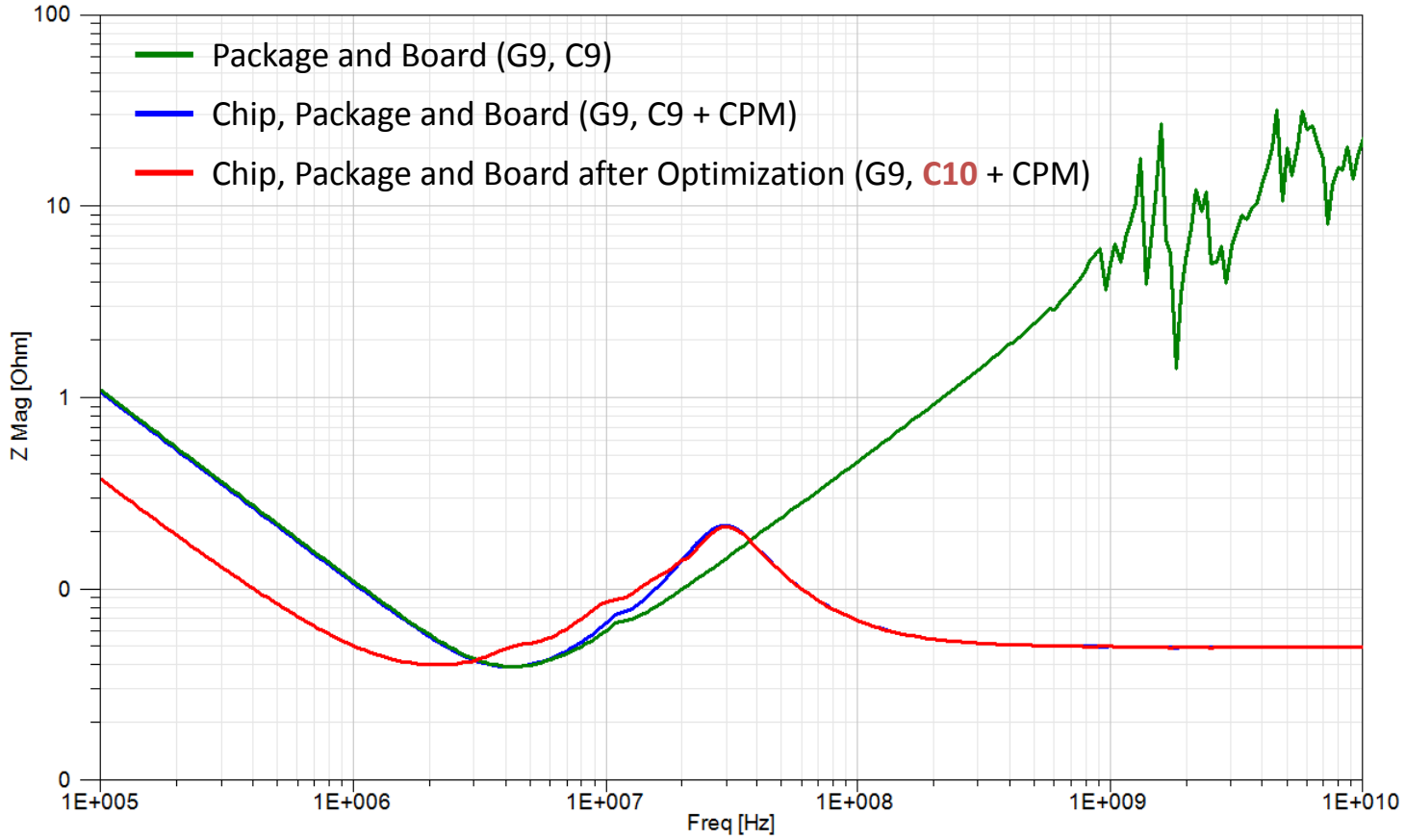
Overview of Simulation :



Bypass Caps Placement (Bottom Layer) / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

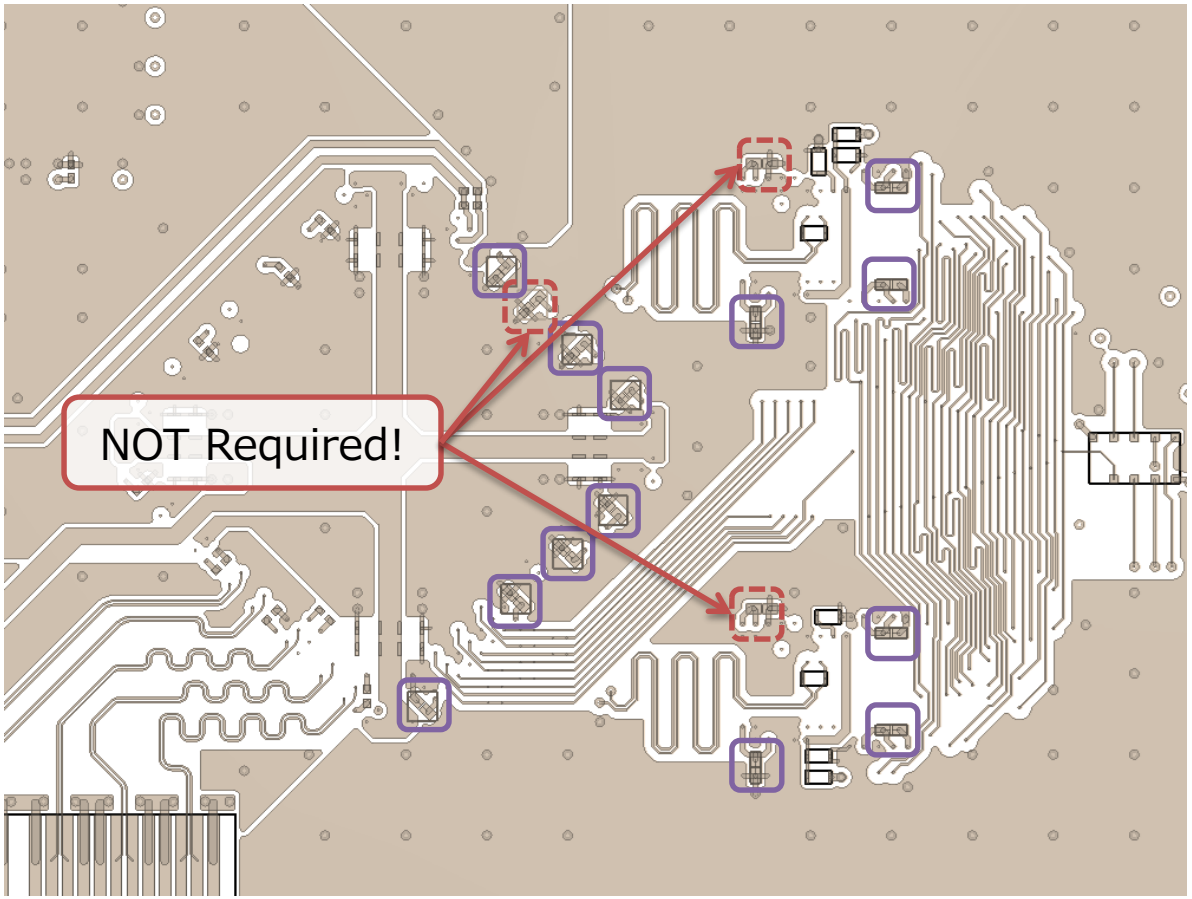
Simulation Result :



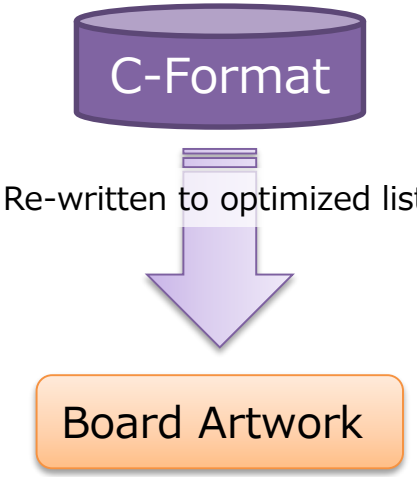
Input Impedance of 1.5V Power on Controller IC / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

Simulation Result :



Bypass Caps Placement (Bottom Layer) / ANSYS SIwave (Extraction Tool)

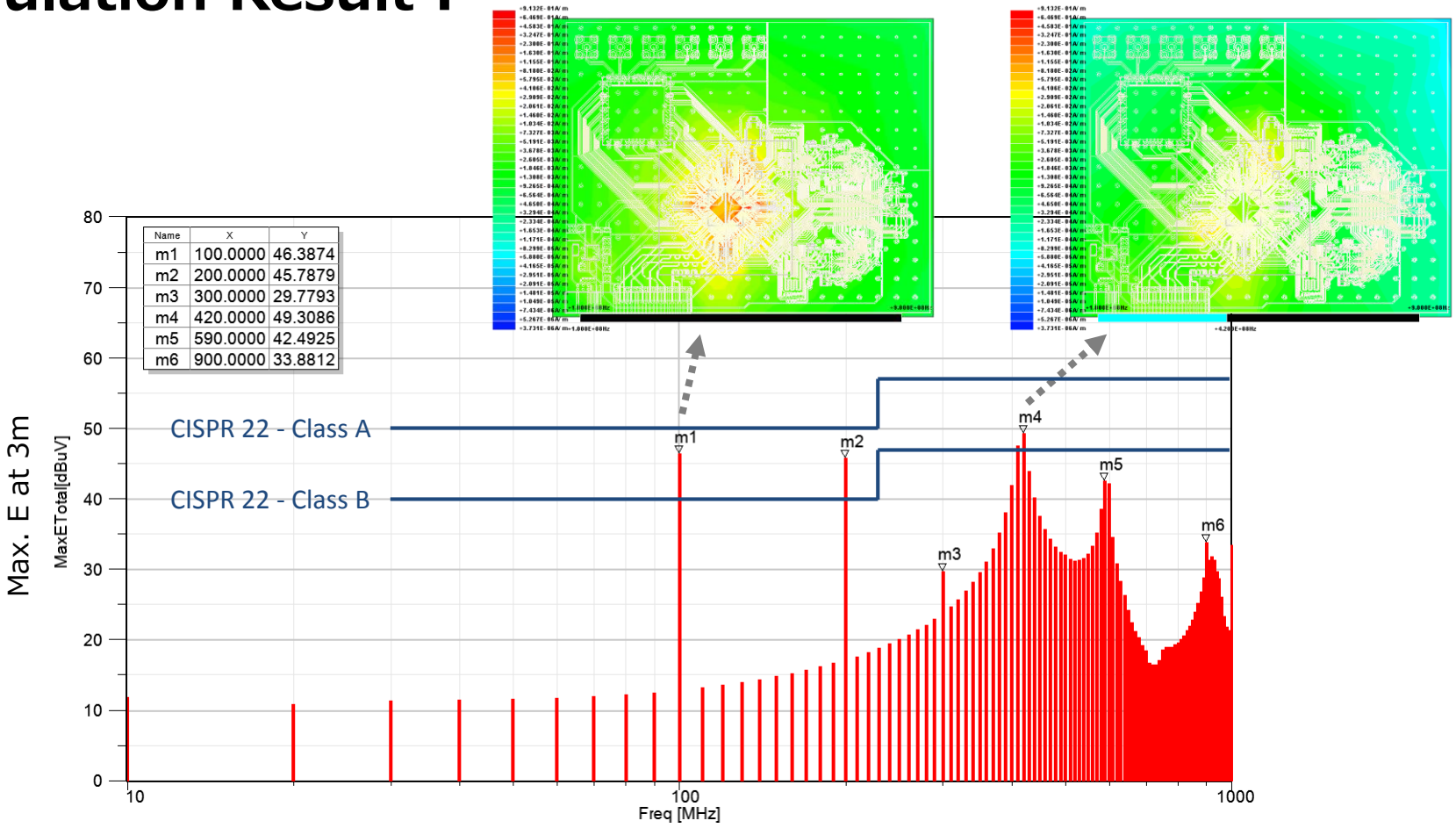


(10) Final Layout Check

Simulation Result :

H-field 1mm above (100MHz)

H-field 1mm above (420MHz)



Far Field and Near Field / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

Works :

(10) Final Layout Check

【Power Integrity Simulation of PDN】

- Input Impedance Analysis of Controller IC and Bypass Caps Optimization
  - ✓ Chip-Package-System Total Impedance ⇒ **OK**
  - ✓ Bypass Caps Optimization ⇒ **Optimized**

【EMI (Far/Near Field) Simulation】

- Far/Near Field analysis induced by Power Noise
  - ✓ CISPR 22 Test (Far Field) ⇒ **OK**
  - ✓ Checks Near Field ⇒ **OK**

LPB Standard Format
Summary

Benefit of LPB format

- **Quick & Accurate design/simulation set up**
  - Enable EMC check from development early stage
  - No more e-mail/phone call/meetings
  - Avoid human error; eliminate hand edit, version control
- **Feedback can be done from any parties, and instantly.**
  - For optimization/cost down/quality up feed back
- **Easy implementation**
  - Human readable, open format XML/Verilog-HDL
  - XML parser available.
  - Simple / light geometry format (G-format:XFL)

Join us!

Visit & Support

- Poster exhibition in B1 floor small hall
- Visit website “LPB format” ”LPB forum”
- Please support International Standard IEEE SA P2401

Link Together by LPB standard format