LSI Package Board needs...

- Mutual Communication
- Design Consistency
- Shorten Development Time

Enabled by New Standard format
Agenda & Speakers

◆ Introduction
  ➢ Yoshinori Fukuba  TOSHIBA

◆ LPB Standard Format
  ➢ Yuji Nakagawa  Fujitsu

◆ EDA - example of design tool
  ➢ Kazunari Koga  Zuken

◆ EDA – example of modeling/simulations
  ➢ Toru Watanabe  ANSYS

◆ Summary : Benefits
  ➢ Yoshinori Fukuba  TOSHIBA
Introduction of Fukuba

- Yoshinori Fukuba
  - Chief specialist, Design Technology Development dept., Mixed Signal IC Dev., TOSHIBA corporation Semiconductor & Storage
  - Chairman JEITA EDA-TC/LSI Package Board(LPB) interoperable design process WG(LPB-WG)
  - Chairman IEEE Standard Association, Computer Society, Design Automation, Project : P2401 LPB-WG
  - Secretary IEC SC47A Integrated circuit
About LPB-WG

Semiconductor board
Electronic Design Automation Technical Committee
LPB(LSI Package board) interoperable design process working group


• Members

• LPB-WG + ex-LPB-WG
  Toshiba, Fujitsu semiconductor, Renesas Electronics
  Canon, Sony, Panasonic, Denso, Nokia
  Fujitsu VLSI, Sony LSI, NEC System Technologies
  Toppan NEC Circuit solutions
  Zuken, Cadence Japan, Mentor Graphic Japan, StayShift(nimbic)
  Fujitsu Advanced Technologies, Gem Design Technologies.
  ANSYS, ANSYS Apache, ATE service(Sigrity)
Issues

• Product development flow & EMC issues

Product planning → Circuit Design → Layout → SI/PI/EMC Check → Manufacturing → Compliance/Field Test

Current → EMC NG

Time consuming, re-design at all => development cost, missing business widow
Target to improve

• How to improve…

- Improve - put check point from early stage,

  Improve

- Reduce iterations
  => Time to market

- EMC issues
  Free
Challenge of EMC simulation in design

- To estimate simulation time which is allowed in each design steps

- Allowable simulation times are different in the development stage.
What is the simulation time?

- **Definition**

Simulation time =

- Parameter collection + setup + calculation
  - Meeting, e-mail, negotiations + hand + mesh, method, hard

**Typical TAT**

- 2 weeks
- 1 day
- 30 hours

**Time**
However...

- Actually ...

Allowable Simulation time

1~3 weeks

EMC simulation cannot be done at early stage.
Challenge to reduce the time. But...

Parameter collection | setup | calculation
--- | --- | ---
Meeting, e-mail, negotiations | hand | mesh, method, hard

2 weeks | 1 day | EDA / computer / Academic challenge

X10~ X100

EDA supplied by OR tech

3D view: Port definition
Test pulse excited at port 11

- Simulation time < 97 sec / port
- Memory usage 680 MB
- 13 Million cells; grid: 15 μm < Δ < 200 μm
- Used CPU: Intel Xeon E5-2687V
Still ...

- Not enough …

Allowable Simulation time

Still …EMC simulation cannot be done at early stage.
What LPB is trying to achieved?

Parameter collection | setup | calculation
--------------------|-------|-------------------
2 weeks | 1 day | EDA / computer / Academic challenge

Common formats

List of information, exchange format, common terms & definitions

Extremely shorten total simulation time

Community / e-commerce

2d - 2 weeks - 1 day - 2 weeks
Reach to the target!

- Finally!

Product planning  Circuit Design  Layout  SI/PI/EMC Check  Manufacturing  Compliance /Field Test

EMC optimization time  EMC verification

1~3 weeks

EMC simulation can be done from early stage.
• LPB Standard forma is also effective to shorten design process.
Design and Simulation

- LPB Standard forma is also intended to shorten design process.

Product planning  Circuit  Layout  SI/PI/EMC Check  Manufacturing  Compliance/Field Test

EMC Check Sim  EMC Check Sim  EMC Check Sim  EMC Check Sim

Quality + Time to market
JEITA LPB-WG produce LPB Standard format.

Design environment to be constructed by 6 formats,
1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary
LPB standard format reveal what the information necessary. The required information must be shared and are provided in the supply chain.
LPB Community

http://www.lpb-forum.com/

● User/EDA/Suppliers community

EDA vendors
- CAD
- CAE
- Develop
- LPB interface

Users/Designers
- Semiconductor
- Electronics products
- Implement
- LPB design flow

Suppliers
- Package, PWB, Passive, Connectors, etc.
- Deliver design rule parametric data
- With LPB format.

LPB Standard format is promoted as for ‘Forum Standard’.

Exhibit

● Show

edsfair

http://www.edsfair.com/

Release/Update

Feedback

● Standardization committee

JEITA EDA-TC/LPB-WG

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International Standardization Plan

- Standardization Plan
  Introduction: DAC2013 2013/6/3-6/5

Submit Project Approval Request (PAR) to IEEE Standard Association @ 2013 Oct.

Approved project: P2401 LPB-WG

Target IEEE standard/IEC dual logo: 2015 June
EDA venders adoption

• More then 10 venders already start to develop LPB interface.
LPB Standard Format & Usage example
Design environment to be constructed by 6 formats

1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary
## LPB Standard Format Abstract

<table>
<thead>
<tr>
<th>Format</th>
<th>Abstract</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| **Project Management**  | Manage the LPB files of the LSI, package and board.  
- Manage the history, revision and update of the files  
- JEITA original format using XML                                                                                                           | Easy to Manage Design history  
Easy to understand Design Status  
Understanding The Latest Condition for Verification                                                                                      |
| **(M-Format)**          |                                                                                                                                                                                                          |                                                                                                                                                                                                       |
| **Netlist**             | Connection of the parts  
- Netlist between LSI, Package and Board.  
- Verilog HDL format                                                                                                                           | Easy to Check Connection Between LSI-PKG-Board  
Enable to Simulate on Board Level                                                                                                              |
| **(N-Format)**          |                                                                                                                                                                                                          |                                                                                                                                                                                                       |
| **Component**           | Information of the parts that includes  
- Pin assignment  
- Design constraint  
- Design Status  
- JEITA original format using XML                                                                                                           | Easy to Verify for Optimization of LPB  
Clarification of Constraint Condition                                                                                                          |
| **(C-Format)**          |                                                                                                                                                                                                          |                                                                                                                                                                                                       |
| **Design Rule**         | Rules of the components that includes  
- Design rule  
- Assembly rule  
- Characteristics of the material  
- JEITA original format using XML                                                                                                           | Clarification of Design Rule in Advance  
Clarification of Verification Condition  
Easy to Set up for Verification                                                                                                               |
| **(R-Format)**          |                                                                                                                                                                                                          |                                                                                                                                                                                                       |
| **Geometry**            | Geometry of the Package and Board  
- XFL format                                                                                                                                  | Efficient Use of Design Property  
Use as Reference Design  
Easy to convert Data                                                                                                                        |
| **(G-Format)**          |                                                                                                                                                                                                          |                                                                                                                                                                                                       |
### Project Manage (M-Format)

<table>
<thead>
<tr>
<th>Abstract</th>
<th>Example</th>
</tr>
</thead>
</table>
| Manage the LPB files of the LSI, package and board.  
- Manage the history, revision and update of the files  
- JEITA original format using XML | <include MFORMAT="MFMT_FKB48.xml" />
<include MFORMAT="MFMT_SOC_PKG.xml" />

<class comment="DDR MEMORY">
  <CFORMAT file_name="CFMT_DDR.xml" />
  <RFORMAT file_name="RFMT_DDR.xml" />
  <NFORMAT file_name="NFMT_DDR.v" />
  <OtherFile file_name="DDRPowerModel.sp" />
</class> |
Netlist (N-Format)

Abstract
Connection of the parts
- Netlist between LSI, Package and Board.
- Verilog HDL format

Example
module JEITA_SAMPLE ( );
    wire [23:0] FKBDO ;
    wire [23:0] FKBDI ;
    wire VDD33 ; /* PG_NET */
    wire DGND ; /* PG_NET */

    FKB48 FKB48 ( .AIN(FKBDO), .AOUT(FKBDI) ) ;
    SOC_PKG SOC ( .FKBDO(FKBDO), .FKBDI(FKBDI) ) ;
endmodule
LPB Standard Format Abstract

Component (C-Format)

<table>
<thead>
<tr>
<th>Abstract</th>
<th>Information of the parts that includes - Pin assignment - Design constraint - Design Status - JEITA original format using XML</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>&lt;module name=&quot;SOC_PKG&quot; type=&quot;PKG&quot; shape_id=&quot;PKG_BODY&quot; &gt; &lt;socket name=&quot;SOC_PKG&quot; &gt; &lt;port id=&quot;A5&quot; x=&quot;-8500&quot; y=&quot;12500&quot; angle=&quot;0&quot; name=&quot;FKBDO[5]&quot; /&gt; &lt;port id=&quot;A6&quot; x=&quot;-7500&quot; y=&quot;12500&quot; angle=&quot;0&quot; name=&quot;FKBDO[2]&quot; /&gt; &lt;constraint&gt; &lt;impedance group_name=&quot;FKB_DIN&quot; type=&quot;single&quot; min=&quot;40&quot; typ=&quot;50&quot; max=&quot;60&quot;/&gt; &lt;delay group_name=&quot;FKB_DIN&quot; min=&quot;100&quot; typ=&quot;150&quot; max=&quot;200&quot; /&gt; &lt;/constraint&gt; &lt;/socket&gt; &lt;/module&gt;</td>
</tr>
</tbody>
</table>

![Diagram of BGA package with socket and skew error](image)
### LPB Standard Format Abstract

#### Design Rule (R-Format)

<table>
<thead>
<tr>
<th>Abstract</th>
<th>Rules of the components</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>- Design rule</td>
</tr>
<tr>
<td></td>
<td>- Assembly rule</td>
</tr>
<tr>
<td></td>
<td>- Characteristics of the material</td>
</tr>
<tr>
<td></td>
<td>- JEITA original format using XML</td>
</tr>
</tbody>
</table>

#### Example

```xml
<material_def>
  <conductor material="COPPER" volume_resistivity="1.68e-8" />
  <dielectric material="FR-4" permittivity="4.5" tan_delta="0.035" />
</material_def>

<layer_def>
  <layer name="TOP_COND" type="conductor" thickness="0.030"
         conductor_material="COPPER" />
  <layer name="DIELECTRIC12" type="dielectric" thickness="0.100"
         dielectric_material="FR-4" />
</layer_def>

<spacing_def>
  <layer name="TOP_COND">
    <line_to_line space="0.050" />
  </layer>
</spacing_def>
```
### Geometry (G-Format)

| Abstract | Geometry of the Package and Board  
- XFL format |
|----------|-----------------------------------|
| Example  | shape 1 4 53.2 26.8 90 N  
via 1 4 V020C060C085 54.55 20 0 N  
via 2 3 B010C050C075C23 41 24.25 0 N  
shape 1 11 35.5 29 0 N  
via 1 2 B010C030C12 35.5 29 0 N  
path 2 0.1 {  
  41 24.25  
  41.000000 24.750000  
} |
LPB Files Delivery

- Die models IBIS/SPICE CPM/LPM
  - C-Format
    - Die Size
    - Pad location
    - Spice Model correspondence
  - Package size
    - Terminal location
    - Spice/IBIS/S-para model correspondence

- Passive components/connectors
  - Simulation model S-para SPICE IBIS

- Die models
  - Die mount rotation
  - Flip
  - Package mount rotation

- Connectivity
  - N-Format
    - Die mount rotation
    - Flip
  - C-Format
    - Package
    - Die size
    - Pad location
    - Spice Model correspondence

- Analysis
  - R-Format
    - Wire Bonding rules
    - Line/Space
    - Via pitch/size/hole
    - Layer Stuck up Material parameter

- M-Format
  - Revision number of Each N/C/R/G files

- G-Format
  - PKG routing
  - Plane
  - Bond wire
  - PWB Routing
  - Plane

- Auto set-up simulation project
LPB sample files for test bench

Golden Sample are provided as a test bench for implementation.
To understand the function of the LPB standard format.
Growth of LPB files in design steps

<table>
<thead>
<tr>
<th>C-Format</th>
<th>Module</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>header</td>
<td>placement</td>
</tr>
<tr>
<td>Global</td>
<td>unit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>shape</td>
<td></td>
</tr>
<tr>
<td></td>
<td>pad stack</td>
<td></td>
</tr>
<tr>
<td></td>
<td>port</td>
<td></td>
</tr>
<tr>
<td></td>
<td>port group</td>
<td></td>
</tr>
<tr>
<td></td>
<td>power domain group</td>
<td></td>
</tr>
<tr>
<td></td>
<td>swappable port/group</td>
<td></td>
</tr>
<tr>
<td></td>
<td>frequency</td>
<td></td>
</tr>
<tr>
<td></td>
<td>constraint</td>
<td></td>
</tr>
<tr>
<td></td>
<td>specification</td>
<td></td>
</tr>
<tr>
<td></td>
<td>reference</td>
<td></td>
</tr>
</tbody>
</table>

**LPB files will grow every time you go through the process of the design.**

Port ID, Coordinate, Port Name

Swappable Ports/Port groups

Impedance, Delay, Skew

Placement Information of the parts

[Example]

```xml
<placement ref_module="SOC" inst="SOC" x="400" y="-6500" />  
<placement ref_module="DDR" inst="DDR0" x="37000" y="-3200" />  
```
<Example> The growth of C-format

LPB files grow and share the information each other.

Coordinate of port only

PKG-C2

Add Name of the port by Board designer

PKG-C3

Dispute?

Change the assignment by Package designer

PKG-C4
<Example> The growth of C-format

PKG-C3

No info. about port swap

PKG-C4

Add swappable info.

Her is additional preparation

Give the constraint from package designer to board designer

Based on the constraint, board designer can change the design

Share the information about constraint and flexibility

=> change of design proposal is possible
Reference Flow Demonstration
Reference flow using LPB standard format

LSI Vendor (Package Design)

- (2) LSI Outline SPEC.
- (4) PKG Pin Assignment
- (6) PKG Pre Layout
- (8) PKG Final Layout

Electric Products Maker

- (1) Block Diagram
- (3) Floor Plan
- (7) Pre Layout Check
- (10) Final Layout Check

Board Artwork

- (5) Board Pre Layout
- (9) Board Final Layout

Substrate/Component Vendors

- ICs DDR, Power IC, etc.
- PWB Substrate
- Passive, Socket, Connector

LSI Requirement

- PKG C2
- PKG N2
- PKG C3
- PKG C4
- PKG C6
- PKG G6
- PKG R6
- PKG C8
- PKG G8

ICs

- ICs C
- ICs N

TOP

- TOP C3
- TOP N3
- TOP C5
- TOP G5
- TOP C7
- TOP N7
- TOP C9
- TOP G9

TOP R
(5) Board Pre Layout

LPB format

Floorplan Result.
Tentative pin assignment is done.

Critical Path Routing

Optimize Placement

LPB format

Add the change of floorplan and pin assignment.
(5) Board  Pre Layout

Change placement info.

<placement y="-8223.2" x="30206.5" mount="TOP" angle="270" z="200" inst="DDR0" ref_module="DDR"/>
<placement y="15911.7" x="36947.6" mount="TOP" angle="270" z="200" inst="DDR1" ref_module="DDR"/>
<placement y="-6500" x="400" mount="TOP" angle="0" z="200" inst="SOC" ref_module="SOC_PKG"/>
<placement y="22417.2" x="-8150.9" mount="TOP" z="20" inst="GRM1_C1" ref_module="GRM1"/>
<placement y="23603.4" x="-4479.3" mount="TOP" z="20" inst="GRM1_C2" ref_module="GRM1"/>

<placement y="-3223.2" x="37206.5" mount="TOP" angle="90" z="200" inst="DDR0" ref_module="DDR"/>
<placement y="10911.7" x="30947.6" mount="TOP" angle="90" z="200" inst="DDR1" ref_module="DDR"/>
<placement y="-6500" x="400" mount="TOP" angle="45" z="200" inst="SOC" ref_module="SOC_PKG"/>
<placement y="22417.2" x="-8150.9" mount="BOTTOM" z="20" inst="GRM1_C1" ref_module="GRM1"/>
<placement y="23603.4" x="-4479.3" mount="BOTTOM" z="20" inst="GRM1_C2" ref_module="GRM1"/>
(5) Board  Pre Layout

Swap pin

<port id="R24" type="signal" y="-1500" x="10500" name="DDRDQ[0]" direction="inout"/>
<port id="R25" type="signal" y="-1500" x="11500" name="DDRDQ[1]" direction="inout"/>
<port id="R26" type="signal" y="-1500" x="12500" name="DDRDQ[2]" direction="inout"/>
<port id="P24" type="signal" y="-500" x="10500" name="DDRDQ[3]" direction="inout"/>
<port id="P25" type="signal" y="-500" x="11500" name="DDRDQ[4]" direction="inout"/>
<port id="P26" type="signal" y="-500" x="12500" name="DDRDQ[5]" direction="inout"/>

<port id="R24" type="signal" y="-1500" x="10500" name="DDRDQ[7]" direction="inout"/>
<port id="R25" type="signal" y="-1500" x="11500" name="DDRDQ[0]" direction="inout"/>
<port id="R26" type="signal" y="-1500" x="12500" name="DDRDQ[2]" direction="inout"/>
<port id="P24" type="signal" y="-500" x="10500" name="DDRDQ[6]" direction="inout"/>
<port id="P25" type="signal" y="-500" x="11500" name="DDRDQ[3]" direction="inout"/>
<port id="P26" type="signal" y="-500" x="12500" name="DDRDQ[4]" direction="inout"/>

PKG  C4

PKG  C5
Simulation Setup

Input for Simulation:

- Board, Package Geometry
- Traces, Vias, Pads
- Planes, Polygons
- etc...

Layout Tools:
- Zuken
- Design Force
- Cadence
- APD
- etc...

G-Format

Extraction Tools:
- ANSYS
- ANSYS SIwave, ANSYS HFSS
- etc...

Package Designed by APD

Board Designed by Design Force
Simulation Setup

Input for Simulation:

- Passive Components
  - C, L, R
- Constraints
  - Skew, Frequency, etc...

Layout Tools:
- Zuken Design Force
- Cadence APD
- etc...

Extraction Tools:
- ANSYS
- ANSYS SIwave, ANSYS HFSS
- etc...

C-Format

Capacitor (C, ESL, ESR)
Inductor (L)
Resistor (R)
(7) Pre Layout Check
(7) Pre Layout Check

Works:

(7) Pre Layout Check

【Signal Integrity Simulation of Critical Nets】

- Timing Verification of DDRIII 1.3GBps Write Cycle
  - Is Damping Resistors required?
  - What is the best ODT setting?
  - Estimate the worst skew of DQ
(7) Pre Layout Check

Geometry:

- Designed by Cadence APD
- All nets are completely routed
- DQs are NOT isometric

- Designed by Zuken Design Force
- Only 1.5V Power, Ground, DQS and DQ
- DQS and DQs are isometric

Merged and stacked in Extraction Tool
(7) Pre Layout Check

Overview of Simulation:

[Controller IC]
- IC: IBIS Model
- Input 666MHz Cycle PRBS to DQ0-7

[DDRIII]
- IC: IBIS Model
- ODT: Test for 30, 40, 60 and 120Ω

DQS, DQ signals in Package and Board Layout / ANSYS SIwave (Extraction Tool)
(7) Pre Layout Check

Simulation Result:

Eye Diagram (ODT : 30Ω (FAIL))

Eye Diagram (ODT : 60Ω (Best Case))

Transient Waveform of DQS and DQ0～7

[Worst Skew (Case of ODT=60Ω)]

- 42.8ps (DQ5-DQ6)

Eye Diagram and Transient Waveform / ANSYS DesignerSI (Circuit Simulator)
(9) Board Final Layout

Import the result of pre layout check
- Skew
- Decap

Re design to satisfy the constraints.
- Change pin assignment
- Change decap

Route other signal
Design power/ground
(10) Final Layout Check

LSI Vendor (Package Design)

(2) LSI Outline SPEC.

(4) PKG Pin Assignment

(6) PKG Pre Layout

(8) PKG Final Layout

Electric Products Maker

(1) Block Diagram

(3) Floor Plan

(7) Pre Layout Check

(9) Board Final Layout

Board Artwork

(5) Board Pre Layout

Substrate/Component Vendors

ICs DDR, Power IC, etc.

ICs C

ICs N

PWB Substrate

Passive, Socket, Connector

Discrete C

Discrete N

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(10) Final Layout Check

Works:

(10) Final Layout Check

【Power Integrity Simulation of PDN】
- Input Impedance Analysis of Controller IC and Bypass Caps Optimization
  - Chip-Package-System Total Impedance
  - Bypass Caps Optimization

【EMI (Far/Near Field) Simulation】
- Far/Near Field analysis induced by Power Noise
  - CISPR 22 Test (Far Field)
  - Checks Near Field
(10) Final Layout Check

Overview of Simulation:

- **Controller IC**
  - IC: CPM (Chip Power Model / Apache RedHawk)
  - Place Port between 1.5V Power and Ground

- **Regulator**
  - DC 1.5V Power Supply

- **Bypass Capacitors**
  - 16 Caps for 1.5V Power

Transient Waveform of 1.5V Power (V vs. T)

Package and Board Layout / ANSYS SIwave (Extraction Tool)
(10) Final Layout Check

Overview of Simulation:

[Bypass Capacitors (Placement)]
- 16 Caps are placed between 1.5V Power and Ground nearby Controller and DDRIII

Bypass Caps Placement (Bottom Layer) / ANSYS SIwave (Extraction Tool)
(10) Final Layout Check

Simulation Result:

Input Impedance of 1.5V Power on Controller IC / ANSYS SIwave (Extraction Tool)
(10) Final Layout Check

Simulation Result:

Bypass Caps Placement (Bottom Layer) / ANSYS SIwave (Extraction Tool)

NOT Required!

C-Format
Re-written to optimized list

Board Artwork
(10) Final Layout Check

Simulation Result:

- H-field 1mm above (100MHz)
- H-field 1mm above (420MHz)

Far Field and Near Field / ANSYS SIwave (Extraction Tool)
(10) Final Layout Check

Works:

(10) Final Layout Check

【Power Integrity Simulation of PDN】

• Input Impedance Analysis of Controller IC and Bypass Caps Optimization
  ✓ Chip-Package-System Total Impedance ⇒ OK
  ✓ Bypass Caps Optimization ⇒ Optimized

【EMI (Far/Near Field) Simulation】

• Far/Near Field analysis induced by Power Noise
  ✓ CISPR 22 Test (Far Field) ⇒ OK
  ✓ Checks Near Field ⇒ OK
LPB Standard Format

Summary
Benefit of LPB format

• Quick & Accurate design/simulation set up
  ➢ Enable EMC check from development early stage
  ➢ No more e-mail/phone call/meetings
  ➢ Avoid human error; eliminate hand edit, version control

• Feedback can be done from any parties, and instantly.
  ➢ For optimization/cost down/quality up feedback

• Easy implementation
  • Human readable, open format XML/Verilog-HDL
  • XML parser available.
  • Simple / light geometry format (G-format: XFL)
Join us!

Visit & Support

- Poster exhibition in B1 floor small hall
- Visit website “LPB format” “LPB forum”
- Please support International Standard IEEE SA P2401

Link Together by LPB standard format